PLESSEY
Semiconductors

SP8685AC

500MHz ÷ 10/11 TWO MODULUS DIVIDER

(CONFORMS TO MIL-STD-883C CLASS B)

The SP8685 is an ECL variable modulus divider, with 10K compatible outputs. It divides by 10 when either of the ECL control inputs, PE1 or PE2 is in the 'high' state and by 11 when both are 'low' (or open circuit).

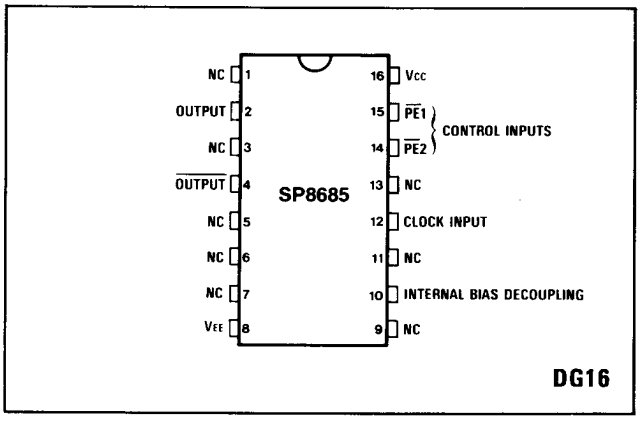


Fig.1 Pin connections - top view

FEATURES

- MIL-M-38510 Change Notification Observed
- Full Quality Conformance Inspection
- Divides by 10 and 11
- AC Coupled Input (Internal Bias)
- ECL Compatible Output
- Power Consumption: 300mV
- Temperature Range: -55°C to +125°C

CHANGE NOTIFICATION

The change notification requirements of MIL-M-38510 will be implemented on this device type. Known customers will be notified of any changes since last buy when ordering further parts if significant changes have been made.

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	-8V
Output current:	20mA
Storage temperature range:	-55° C to +150° C
Max. junction temperature:	+175° C
Max. clock I/P voltage:	2.5V p-p

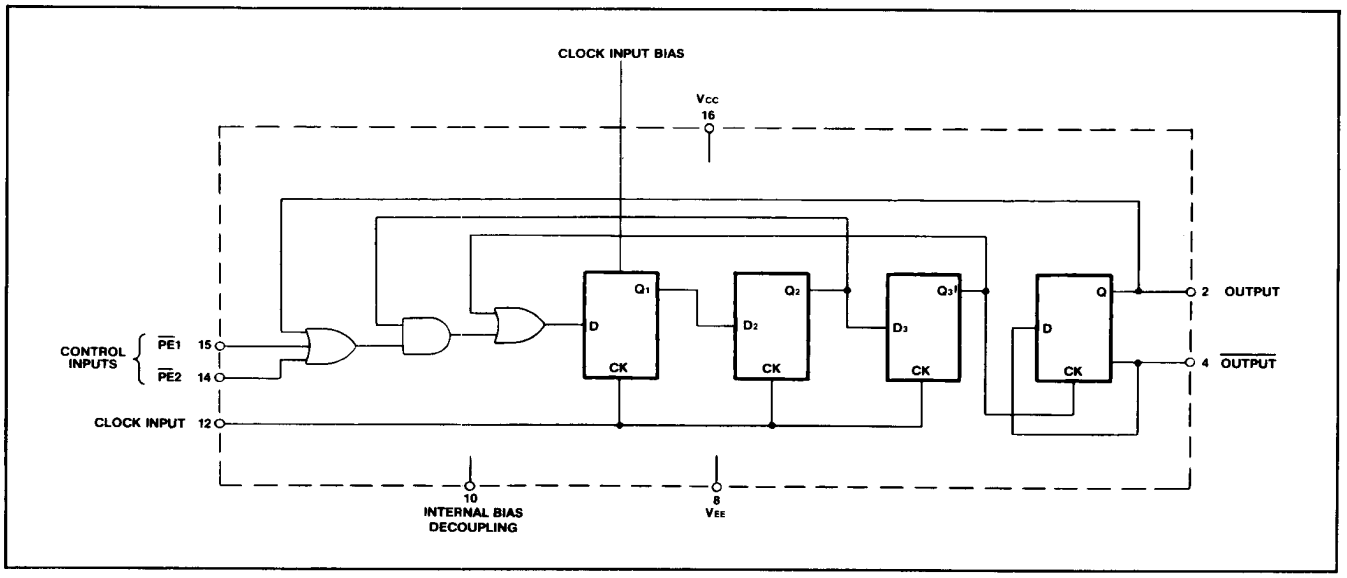


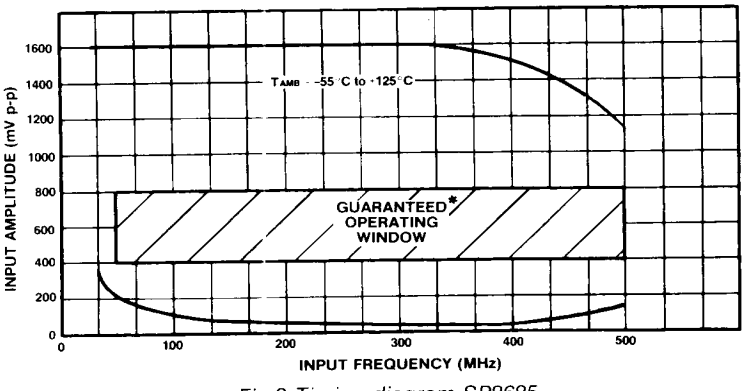
Fig.2 Functional diagram SP8685

Rev.	A		
Date	22 Sept 86		

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Value		Sub group	Notes	Method/Conditions/Temp.
		Min.	Max.			
Operating frequency range	f_{max}	50MHz	500MHz	9,10,11	-	Input = 400mV p-p to 800mV p-p V_{EE} = -5.45V to -4.95V T_{amb} = -55°C to +125°C
Function test		-	-	7,8	Note 1	V_{EE} = -5.20V T_{amb} = -55°C to +125°C
Power supply current	I_{EE}	-	70mA	1,2,3	-	V_{EE} = -5.2V T_{amb} = -55°C to +125°C
ECL output high voltage	V_{OH}	-0.85V	-0.7V	1	-	V_{EE} = -5.2V T_{amb} = +25°C
ECL output high voltage	V_{OH}	-0.73V	-0.50V	2	-	V_{EE} = -5.2V T_{amb} = +125°C
ECL output high voltage	V_{OH}	-1.01V	-0.8V	3	-	V_{EE} = -5.2V T_{amb} = -55°C
ECL output low voltage	V_{OL}	-1.8V	-1.5V	1	-	V_{EE} = -5.2V T_{amb} = +25°C
ECL output low voltage	V_{OL}	-1.73V	-1.38V	2	-	V_{EE} = -5.2V T_{amb} = +125°C
ECL output low voltage	V_{OL}	-1.90V	-1.56V	3	-	V_{EE} = -5.2V T_{amb} = -55°C
$\overline{PE}$ input high voltage	V_{INH}	-0.93V	-	1	Note 2	V_{EE} = -5.2V T_{amb} = +25°C
$\overline{PE}$ input high voltage	V_{INH}	-0.78V	-	2	Note 2	V_{EE} = -5.2V T_{amb} = +125°C
$\overline{PE}$ input high voltage	V_{INH}	-1.00V	-	3	Note 2	V_{EE} = -5.2V T_{amb} = -55°C
$\overline{PE}$ input low voltage	V_{INL}	-	-1.62V	1	Note 2	V_{EE} = -5.2V T_{amb} = +25°C
$\overline{PE}$ input low voltage	V_{INL}	-	-1.53V	2	Note 2	V_{EE} = -5.2V T_{amb} = +125°C
$\overline{PE}$ input low voltage	V_{INL}	-	-1.74V	3	Note 2	V_{EE} = -5.2V T_{amb} = -55°C

NOTES
1. This test is carried out in conjunction with static tests (sub group 1, 2 or 3) and is sufficient to verify the truth table.
2. $\overline{PE}$ input levels are the voltages applied to the $\overline{PE}$ inputs during the function test.
3. Sub groups 4, 5, 6 are not required.



*Tested as specified in table of Electrical Characteristics

Fig.3 Timing diagram SP8685

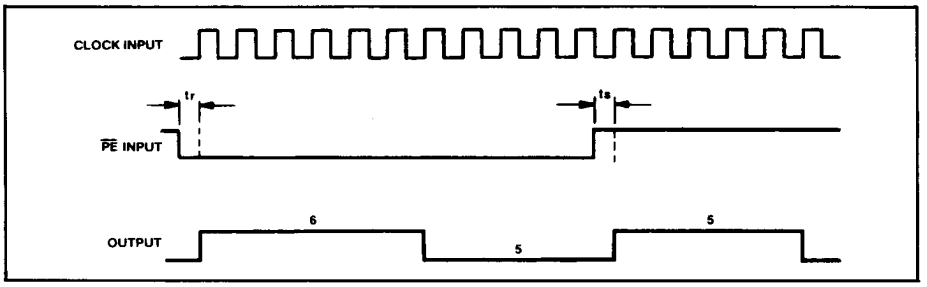


Fig.4 Typical input characteristics SP8685

NOTE:
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of a control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from clock input (Pin 12) to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig.7.
5. The PE inputs are ECL III/10K compatible and include a 4.3k internal pulldown resistor. Unused inputs can therefore be left open.

TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

6. Input impedance is a function of frequency. See Fig.5.
7. All components should be suitable for the frequency in use.

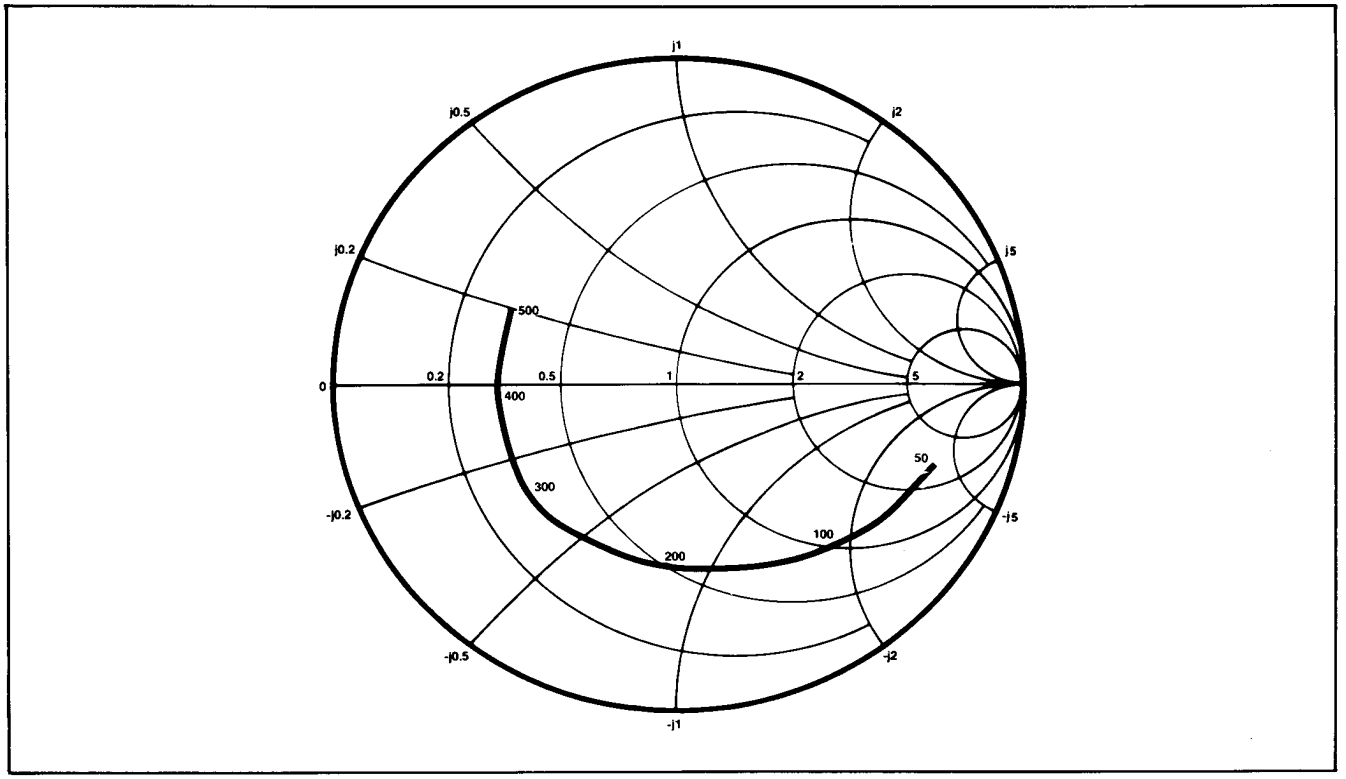


Fig.5 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

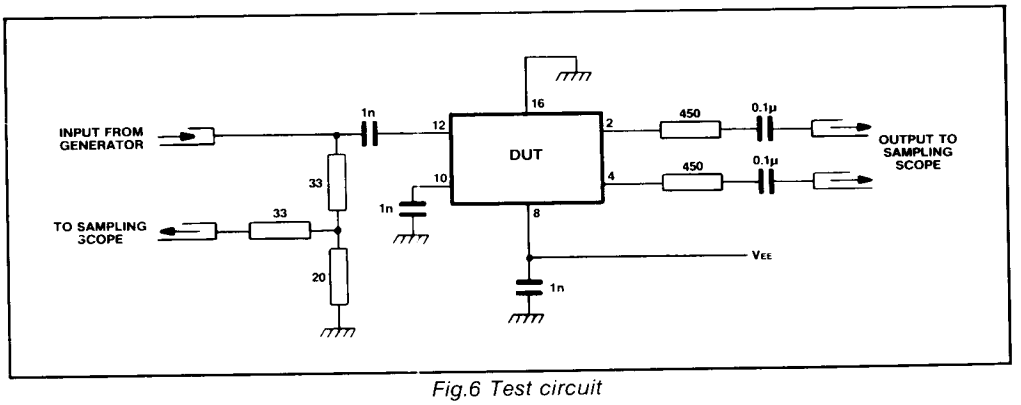


Fig.6 Test circuit

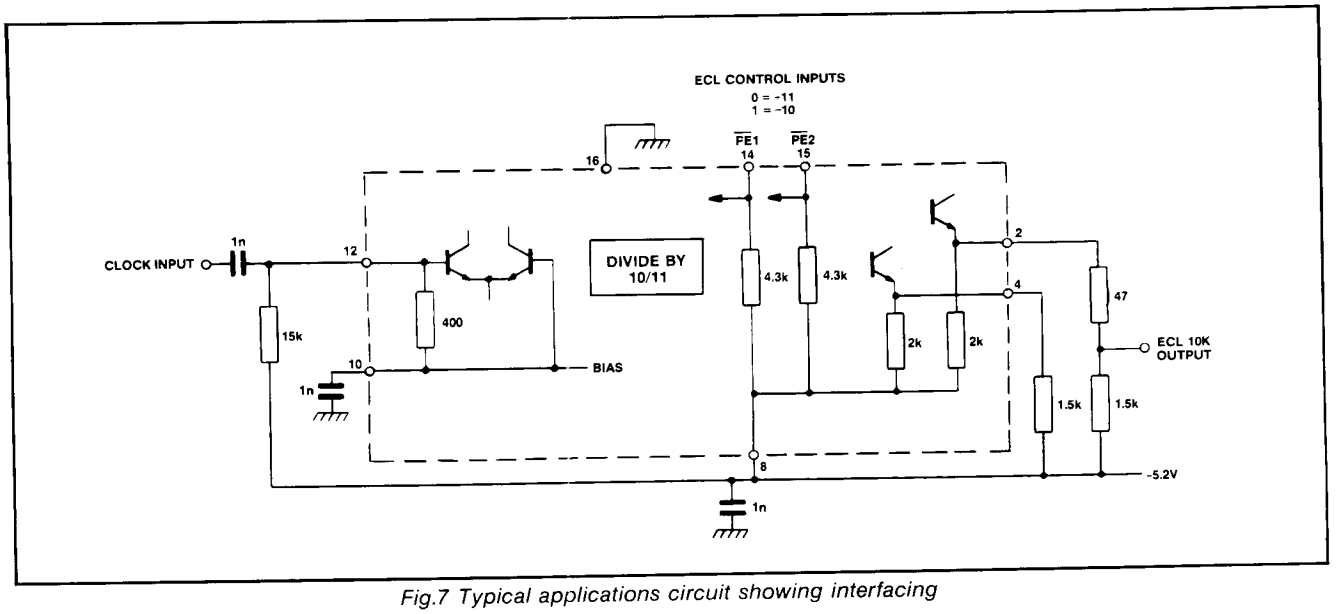


Fig.7 Typical applications circuit showing interfacing

GUARANTEED CHARACTERISTICS

The following characteristics are guaranteed, but not tested, for the SP8685AC at +25° C and over the full supply voltage range (-4.95V to +5.45V).

Parameter	Symbol	Value		Test conditions
		Min.	Max.	
Set-up time	t_s	2ns	-	
Release time	t_r	2ns	-	
Clock to ECL delay (+VE going)	t_p	-	6ns	$I_{OUT} = 0$

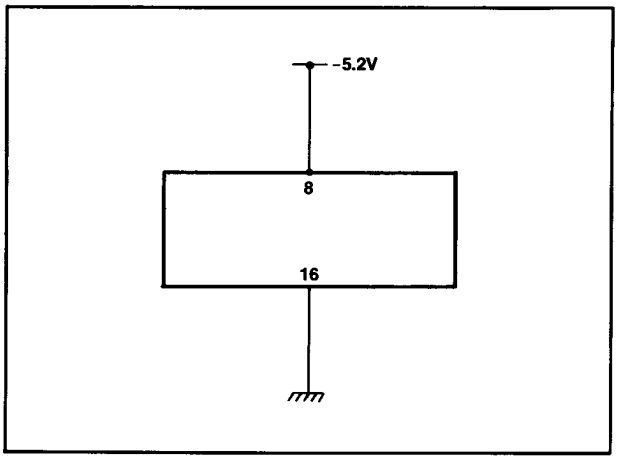


Fig.8 Burn-in/Life test circuit
NOTES (1) The device self-oscillates under above test condition
(2) PDA is 5% and based on sub groups 1 and 7