Monolithic Video A/D Converter

8-Bit, 20Msps

The TRW TDC1048 is a 20Msps (MegaSample Per Second) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 7MHz into 8-bit digital words. A sample-and-hold circuit is not necessary. Low power consumption eases thermal considerations, and board space is minimized with a 28 pin package. All digital inputs and outputs are TTL compatible.

The TDC1048 consists of 255 clocked latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

Features

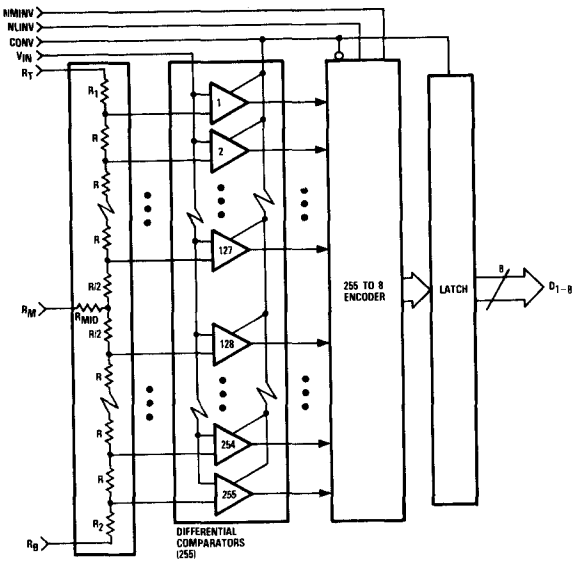
- 8-Bit Resolution
- 20Msps Conversion Rate
- Sample-And-Hold Circuit Not Required
- Differential Phase 1 Degree
- Differential Gain 2%
- 1/2 LSB Linearity
- Guaranteed Monotonic
- TTL Compatible Outputs
- Selectable Data Format
- Available In 28 Pin Plastic DIP, CERDIP, Or LCC
- MIL-STD-883 Compliant Screening Available
- Available Per Standard Military Drawing
- Evaluation Board – TDC1048E1C
- Also Available As A Complete Hybrid – THC1068

Applications

- Low-Cost Video Digitizing
- Radar Data Conversion
- Data Acquisition
- Medical Imaging

A

Functional Block Diagram



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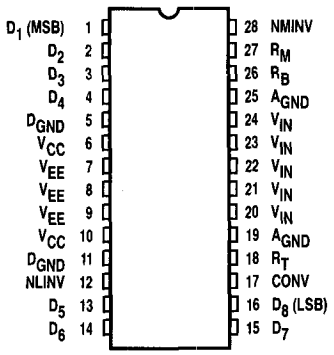
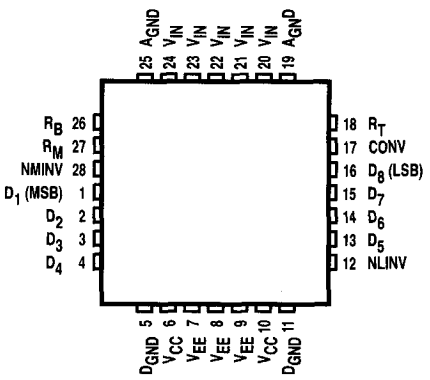
Pin Assignments



28 Pin CERDIP – B6 Package
28 Pin Plastic DIP – N6 Package



28 Contact Chip Carrier – C3 Package
28 Leaded Plastic Chip Carrier – R3 Package

Functional Description

General Information

The TDC1048 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 255 reference voltages to produce an N-of-255 code (sometimes referred to as a "thermometer" code, as all the comparators below the signal will be on, and all those above the signal will be off). The encoding logic converts the N-of-255 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output latch holds the output constant between updates.

Power

The TDC1048 operates from two supply voltages, +5.0V and −5.2V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return for I_{EE}, the current drawn from the −5.2V supply, is A_{GND}. All power and ground pins must be connected.

Reference

The TDC1048 converts analog signals in the range $V_{RB} \leq V_{IN} \leq V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and −2.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 1.8V and 2.2V. The nominal voltages are V_{RT} = 0.0V, V_{RB} = −2.0V.

A midpoint tap, R_M, allows the converter to be adjusted for optimum linearity, although adjustment is not necessary to meet the linearity specification. It can also be used to achieve a nonlinear transfer function. The circuit shown in ***Figure 5*** will provide approximately 1/2 LSB adjustment of the linearity midpoint. The characteristic impedance seen at this node is approximately 220Ω, and should be driven from a low-impedance source. Note that any load applied to this node will affect linearity, and noise introduced at this point will degrade the quantization process.

Due to the variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically, (as in an automatic gain control circuit), a low-impedance reference source is required. The reference voltages may be varied dynamically up to 5MHz.

Control

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. These pins are active LOW, as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Convert

The TDC1048 requires a convert (CONV) signal. A sample is taken (the comparators are latched) within 15ns after a rising edge on the CONV pin. This time is t_{STO}, Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a function of temperature, but the short-term uncertainty (jitter) in sampling offset time is less than 100 picoseconds. The 255 to 8 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. Data is held valid at the output register for at least t_{HO}, Output Hold Time, after the rising edge of CONV. New data becomes valid after a Digital Output Delay, t_D, time. This permits the previous conversion result to be acquired by external circuitry at that rising edge, i.e., data for sample N is acquired by the external circuitry while the TDC1048 is taking input sample N+2.

Analog Input

The TDC1048 uses strobed latching comparators which cause the input impedance to vary with the signal level, as comparator input transistors are cut-off or become active. As a result, for optimal performance, the source impedance of the driving device must be less than 25Ω. The input signal will not damage the TDC1048 if it remains within the range of V_{EE} to +0.5V. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 255 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction. All five analog input pins must be connected together.

Outputs

The outputs of the TDC1048 are TTL compatible, capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONVert signal. For optimum performance, 2.2 kΩ pull-up resistors are recommended.

Package Interconnections

Signal Type	Signal Name	Function	Value	B6, N6, C3, R3 Package Pins
Power	V_{CC}	Positive Supply Voltage	+5.0V	6, 10
	V_{EE}	Negative Supply Voltage	−5.2V	7, 8, 9
	D_{GND}	Digital Ground	0.0V	5, 11
	A_{GND}	Analog Ground	0.0V	19, 25
Reference	R_T	Reference Resistor (Top)	0.0V	18
	R_M	Reference Resistor (Middle)	−0.996V	27
	R_B	Reference Resistor (Bottom)	−2.0V	26
Controls	NMINV	Not Most Significant Bit INVert	TTL	28
	NLINV	Not Least Significant Bit INVert	TTL	12
Convert	CONV	Convert	TTL	17
Analog Input	V_{IN}	Analog Signal Input	0V to −2V	20, 21, 22, 23, 24

Package Interconnections (cont.)

Signal Type	Signal Name	Function	Value	B6, N6, C3, R3 Package Pins
Outputs	D_1	MSB Output	TTL	1
	D_2		TTL	2
	D_3		TTL	3
	D_4		TTL	4
	D_5		TTL	13
	D_6		TTL	14
	D_7		TTL	15
	D_8	LSB Output	TTL	16

Figure 1. Timing Diagram

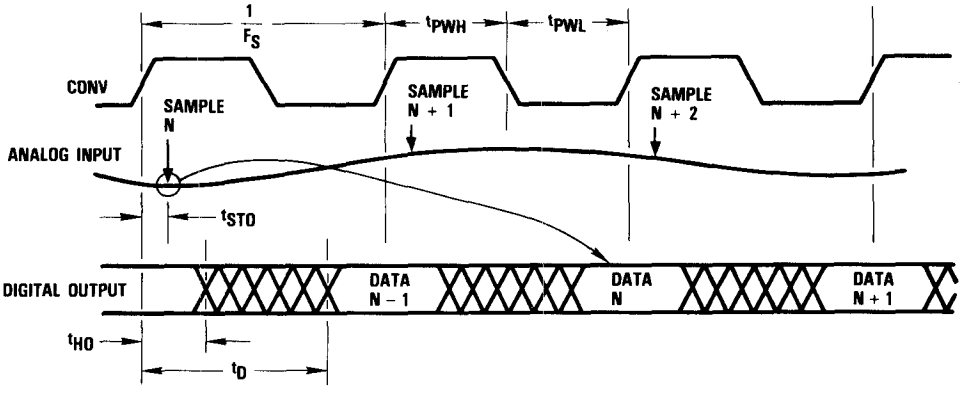
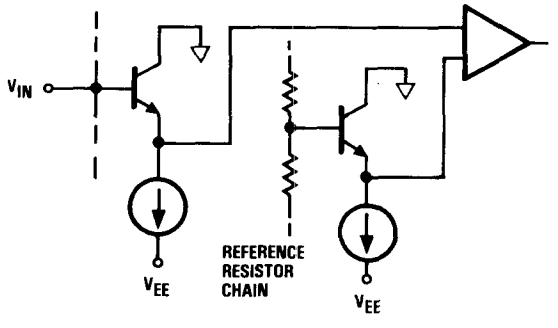
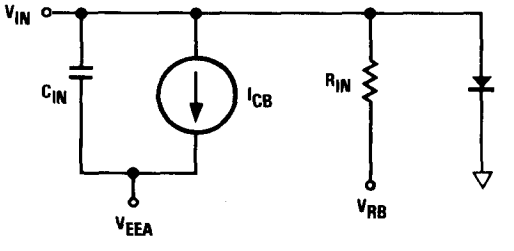


Figure 2. Simplified Analog Input Equivalent Circuit





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

Figure 3. Convert Input Equivalent Circuit

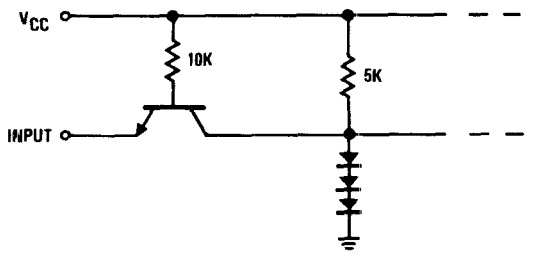
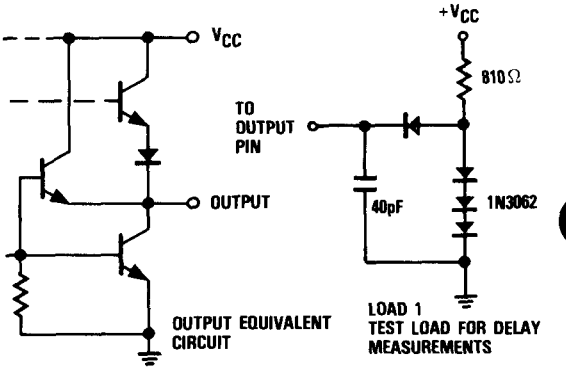


Figure 4. Output Circuits



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Output Coding Table

Step	Range		Binary		Offset Two's Complement	
			True	Inverted	True	Inverted
	−2.0000V FS	−2.0480V FS	NMINV=1	0	0	1
	7.8431mV Step	8.000mV Step	NLINV=1	0	1	0
000	0.0000V	0.0000V	00000000	11111111	10000000	01111111
001	−0.0078V	−0.0080V	00000001	11111110	10000001	01111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
127	−0.9961V	−1.0160V	01111111	10000000	11111111	00000000
128	−1.0039V	−1.0240V	10000000	01111111	00000000	11111111
129	−1.0118V	−1.0320V	10000001	01111110	00000001	11111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
254	−1.9921V	−2.0320V	11111110	00000001	01111110	10000001
255	−2.0000V	−2.0400V	11111111	00000000	01111111	10000000

Notes:
1. NMINV and NLINV are to be considered DC controls. They may be tied to +5V for a logical "1" and tied to ground for a logical "0."
2. Voltages are code midpoints when calibrated by the procedure given below.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND}) ..... −0.5 to +7.0V
V_{EE} (measured to A_{GND}) ..... +0.5 to −7.0V
A_{GND} (measured to D_{GND}) ..... −0.5 to +0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND}) ..... −0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND}) ..... +0.5 to V_{EE}
V_{RT} (measured to V_{RB}) ..... +2.2 to −2.2V

Output

Applied voltage (measured to D_{GND}) ..... −0.5 to +5.5V [2]
Applied current, externally forced ..... −1.0 to +6.0mA [3,4]
Short circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, ambient ..... −55 to +125°C
junction ..... +175°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage	4.75	5.0	5.25	4.50	5.0	5.50	V
V_{EE}	Negative Supply Voltage	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0	+0.1	−0.1	0	+0.1	V
t_{PWL}	CONV Pulse Width, LOW	18			18			ns
t_{PWH}	CONV Pulse Width, HIGH	22			22			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
V_{RT}	Most Positive Reference Input [1]	−0.1	0.0	0.1	−0.1	0.0	+0.1	V
V_{RB}	Most Negative Reference Input [1]	−1.9	−2.0	−2.1	−1.9	−2.0	−2.1	V
V_{RT}-V_{RB}	Voltage Reference Differential	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note: 1. V_{RT} Must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = Max, static [1]		35		40	mA
I_{EE}	Negative Supply Current	V_{EE} = Max, static [1]					
		T_A = 0°C to 70°C		−260			mA
		T_A = 70°C		−185			mA
		T_C = −55°C to 125°C				−320	mA
		T_C = 125°C				−180	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = Nom		40		50	mA
R_{REF}	Total Reference Resistance		50		40		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}	10		10		kOhms
C_{IN}	Input Capacitance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}		100		100	pF
I_{CB}	Input Constant Bias Current	V_{EE} = Max		200		550	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_I = 0.5V					
		CONV		−0.4		−0.4	mA
		NMINV, NLINV		−0.6		−0.6	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = Max, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = Max, Output HIGH, one pin to ground, one second duration max.		−30		−30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note: 1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC} = Min, V_{EE} = Min	20		20		Msps
t_{STO}	Sampling Time Offset	V_{CC} = Min, V_{EE} = Min	0	10	0	15	ns
t_D	Digital Output Delay	V_{CC} = Min, V_{EE} = Min, Load 1		30		35	ns
t_{HO}	Digital Output Hold Time	V_{CC} = Max, V_{EE} = Max, Load 1	5		5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB} = Nom		0.2		0.2	%
E_{LD}	Linearity Error Differential			0.2		0.2	%
CS	Code Size		25	175	25	175	% Nominal
E_{OT}	Offset Error, Top	$V_{IN}=V_{RT}$		+40		+40	mV
E_{OB}	Offset Error, Bottom	$V_{IN}=V_{RB}$		−30		−30	mV
T_{CO}	Offset Error, Temperature Coefficient			±20		±20	μV/°C
BW	Bandwidth, Full Power Input		7		5		MHz
t_{TR}	Transient Response, Full-Scale			20		20	ns
SNR	Signal-to-Noise Ratio	20Msps Conversion Rate, 10MHz Bandwidth					
	Peak Signal/RMS Noise	1.248MHz Input	54		53		dB
		2.438MHz Input	53		52		dB
	RMS Signal/RMS Noise	1.248MHz Input	45		44		dB
		2.438MHz Input	44		43		dB
E_{AP}	Aperture Error			60		60	ps
DP	Differential Phase Error	F_S = 4 x NTSC		1.0		1.0	Degree
DG	Differential Gain Error	F_S = 4 x NTSC		2.0		2.0	%
NPR	Noise Power Ratio	DC to 8MHz White Noise Bandwidth 4 Sigma Loading 1.248MHz Slot 20Msps Conversion Rate	36.5		36.5		dB

Calibration

To calibrate the TDC1048, adjust V_{RT} and V_{RB} to set the 1st and 255th thresholds to the desired voltages. Note that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −2V desired range, continuously strobe the converter with −0.0039V (1/2 LSB from 0V) on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −1.996V (1/2 LSB from −2V) and adjust V_{RB} for toggling between codes 62 and 63.

The degree of required adjustment is indicated by the offset error, E_{OT} and E_{OB}. Offset errors are generated by the inherent parasitic resistance between the package pin and the actual resistor chain on the integrated circuit. These parasitic resistors are shown as R_1 and R_2 in the *Functional Block Diagram*. Calibration will cancel all offset voltages, eliminating offset and gain errors.

The above method of calibration requires that both ends of the resistor chain, R_T and R_B, are driven by buffered operational amplifiers. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error, which can be compensated for by varying the voltage applied to R_B. The bottom reference is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in *Figure 6*.

Typical Interface

Figure 6 shows an example of a typical interface circuit for the TDC1048. The analog input amplifier is a bipolar wideband operational amplifier, which is used to directly drive the A/D converter. Bipolar inputs may be accommodated by adjusting the offset control. TRW's TDC4611 provides a stable reference for both the offset and gain control. All five V_{IN} pins are connected close to the device package, and the buffer amplifier feedback loop should be closed at that point. The buffer has a gain of minus two, increasing a 1Vp-p video input signal to the recommended 2Vp-p input for the A/D converter. Proper decoupling is recommended for all systems.

The bottom reference voltage, V_{RB}, is supplied by an inverting amplifier on the TDC4611, buffered with a PNP transistor. The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain. The bottom reference voltage can be adjusted to cancel the gain error introduced by the offset voltage, E_{OB}, as discussed in the *Calibration* section.

Figure 5. Typical Reference Midpoint Adjust Circuit

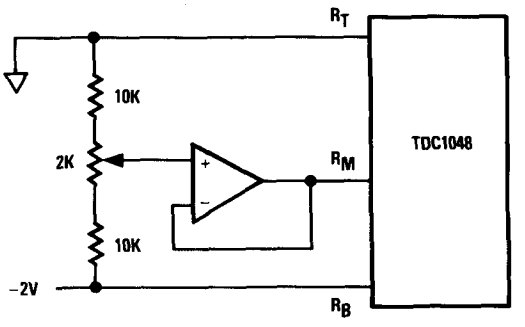
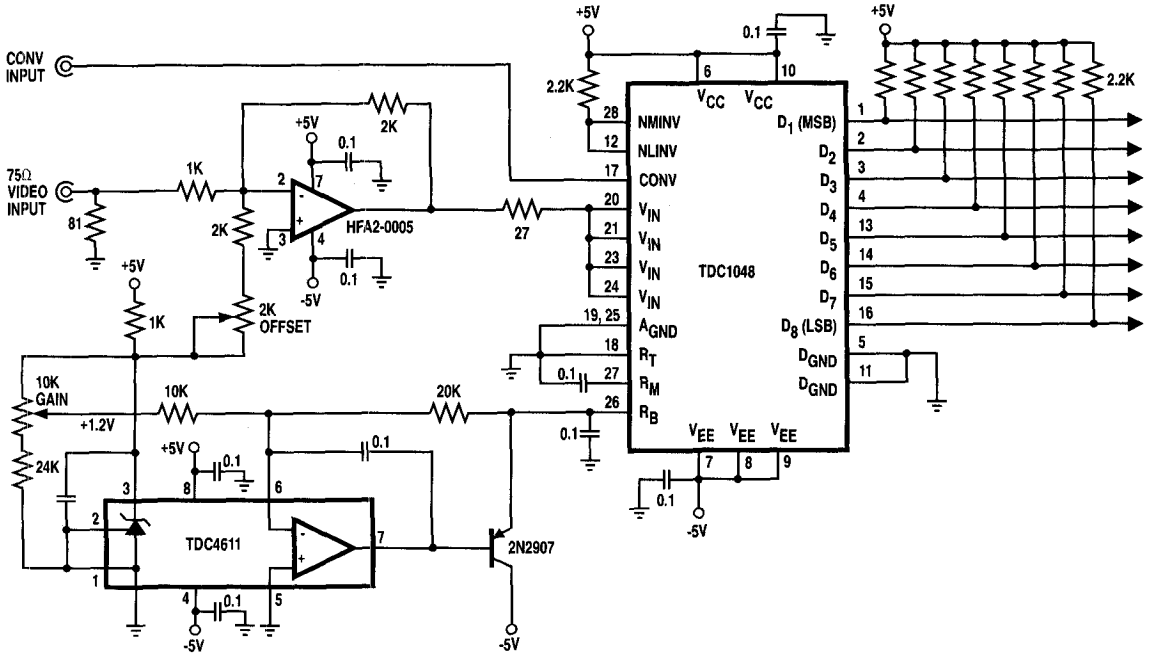


Figure 6. Typical Interface Circuit



Evaluation Board

The TDC1048E1C is a Eurocard-style printed circuit board designed to optimize the performance of, and to aid in the evaluation of, the TDC1048 A/D converter. The board dimensions are 100mm x 160mm with a standard 64 pin double-row DIN male connector installed. A complementary 64 pin double-row DIN female connector is included with the board. The circuitry on the board includes reference voltage generator, wideband video input amplifier, and TDC1048 8-bit A/D converter.

The board employs only two conducting sides. Most of the circuit interconnections are on the bottom of the board while the top is mostly solid ground plane. SMA connectors are installed on the board to facilitate analog I/O and clocks. The board is calibrated and tested at the factory.

Power and Ground

Two power supply voltages are required for the operation of the TDC1048E1C: $V_{CC} = +5V$ and $V_{EE} = -5.2V$. All power inputs are decoupled to a solid ground planes, A_{GND} and D_{GND}. For best performance, all A_{GND} ad D_{GND} pins of the board are connected to power supply ground and all ground pins be should be used.

Voltage Reference Generator

The TDC1048E1C has a voltage reference generator circuit for driving the RB terminal of the TDC1048. With RT grounded, a variable $-2V$ is supplied to RB from U3 and Q1. The GAIN potentiometer provides $\pm 10\%$ adjustment range on the RB voltage. Diodes D1 through D4 act as clamps which protect the TDC1048 from power-on conditions that might violate absolute maximum ratings and damage the TDC1048.

Video Input Amplifier

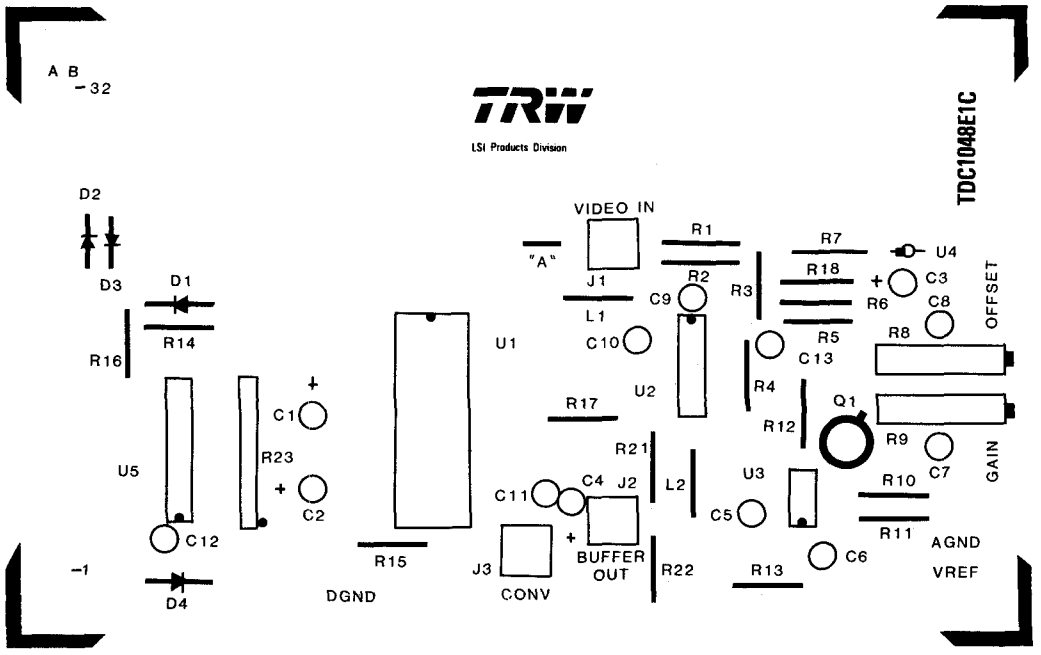
The input amplifier of the TDC1048E1C, U2, has been designed to accept a $\pm 0.5V$ input range and translate that signal to the 0V to $-2V$ range of the TDC1048. The output of this amplifier can be monitored at the J2 SMA connector which is connected to the V_{IN} terminals of the TDC1048 through a 470Ω resistor. The OFFSET potentiometer, R29, gives a $\pm 0.5V$ offset adjustment range to the board.

A/D Converter Inputs

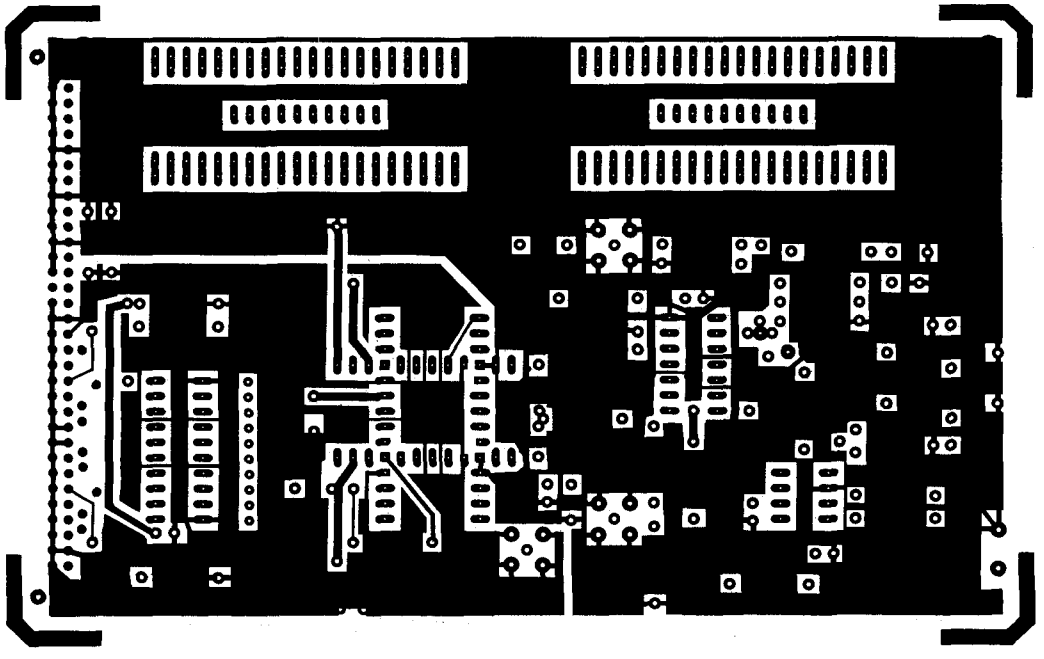
The clock to the TDC1048, CONV, is normally brought onto the board through the SMA connector labeled "CONV." It is also routed to the edge connector pin B15. The NMINV and NLINV inputs to the TDC1048 are pulled HIGH with resistors R14 and R15 and are routed to edge connector pins B13 and B6.

The analog signal input to the TDC1048E1C is brought onto the board by way of the SMA connector labeled "A_{IN}" near pin 28 of the TDC1048. A terminating resistor network, R1 and R2, is included on the board for terminating analog input signal cable. The eight data outputs of the TDC1048 are brought to edge connector pins after registering data in U5.

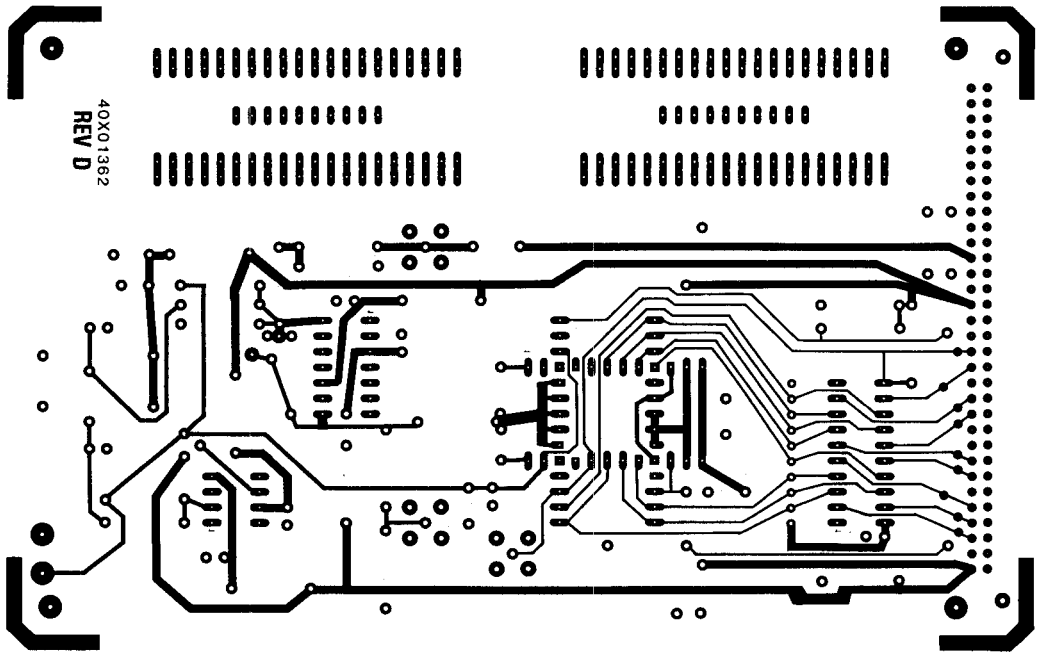
TDC1048E1C Silkscreen Layout



TDC1048E1C Component Side Layout



TDC1048E1C Circuit Side Layout



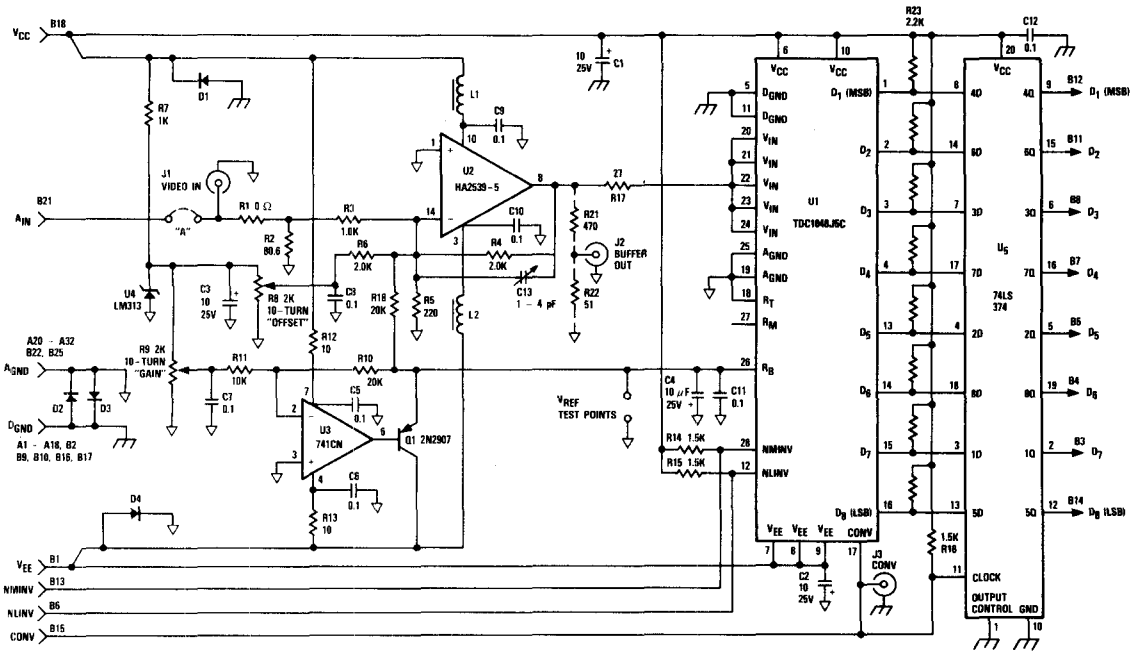
TDC1048E1C Eurocard Edge Connector Pinout

A_{GND}	A32	B32	NC
A_{GND}	A31	B31	NC
A_{GND}	A30	B30	NC
A_{GND}	A29	B29	NC
A_{GND}	A28	B28	NC
A_{GND}	A27	B27	NC
A_{GND}	A26	B26	NC
A_{GND}	A25	B25	A_{GND}
A_{GND}	A24	B24	NC
A_{GND}	A23	B23	NC
A_{GND}	A22	B22	A_{GND}
A_{GND}	A21	B21	A_{IN}
A_{GND}	A20	B20	NC
NC	A19	B19	NC
D_{GND}	A18	B18	V_{CC}
D_{GND}	A17	B17	D_{GND}
D_{GND}	A16	B16	D_{GND}
D_{GND}	A15	B15	CONV
D_{GND}	A14	B14	D8 LSB
D_{GND}	A13	B13	NMINV
D_{GND}	A12	B12	D_1 MSB
D_{GND}	A11	B11	D_2
D_{GND}	A10	B10	D_{GND}
D_{GND}	A9	B9	D_{GND}
D_{GND}	A8	B8	D_3
D_{GND}	A7	B7	D_4
D_{GND}	A6	B6	NLINV
D_{GND}	A5	B5	D_5
D_{GND}	A4	B4	D_6
D_{GND}	A3	B3	D_7
D_{GND}	A2	B2	D_{GND}
D_{GND}	A1	B1	V_{EE}

Mating Connectors for TDC1048E1C

AMP	532507-2	Wire-wrap
AMP	532507-1	Solder tail
Robinson-Nugent	RNE-64BS-W-TG30	Wire-wrap
Robinson-Nugent	RNE-64BS-S-TG30	Solder tail
Souriau	8609-264-6115-7550E1	Wire-wrap
Souriau	8609-264-6114-7550E1	Solder tail
Souriau	8609-264-6813-7550E1	Solder tail, right-angle bend

Figure 7. Schematic of Evaluation Board



Notes for Figure 7. Schematic of Evaluation Board

1. All capacitor values are in microfarads (μF).
2. All capacitor voltage ratings are 50WVDC unless otherwise noted.
3. All resistors are 1/8W unless otherwise noted.
4. All resistor values are in Ohms.
5. All diodes are 1N4001.

Miscellaneous Evaluation Board Parts

Eurocard Connector DIN 41612B 2-Row 64-Contact Board Mount Male	Winchester 64P-6033-0430
Eurocard Connector DIN 41612B 2-Row 64-Contact Wire-Wrap Female	Winchester 64S-6033-0422-1
J1-J3 SMA Coax Connector (J2, J3 not included)	Sealectro 50-651-0000-31 or Omni-Spectra 2062-0000-00
L1, L2 Ferrite Bead Inductors	Fair-Rite Products Corp. 2743001112

Input Resistor Selection Table (Values in Ohms)

Z_{IN}	Input Voltage Range									
	1V		2V		4V		5V		10V	
	R1	R2	R1	R2	R1	R2	R1	R2	R1	R2
50	0	52.3	24.9	24.3	37.4	12.7	40.2	10	45.3	4.99
75	0	80.6	37.4	39.2	56.2	19.1	60.4	15.4	68.1	7.5
93	0	102	46.4	48.7	69.8	23.7	75	19.1	84.5	9.31
1k	0	Open	499	1k	750	332	806	249	909	110

For input voltage ranges and input impedances not covered by the *Input Resistor Selection Table*, the following formulas may be used to calculate R1 and R2:

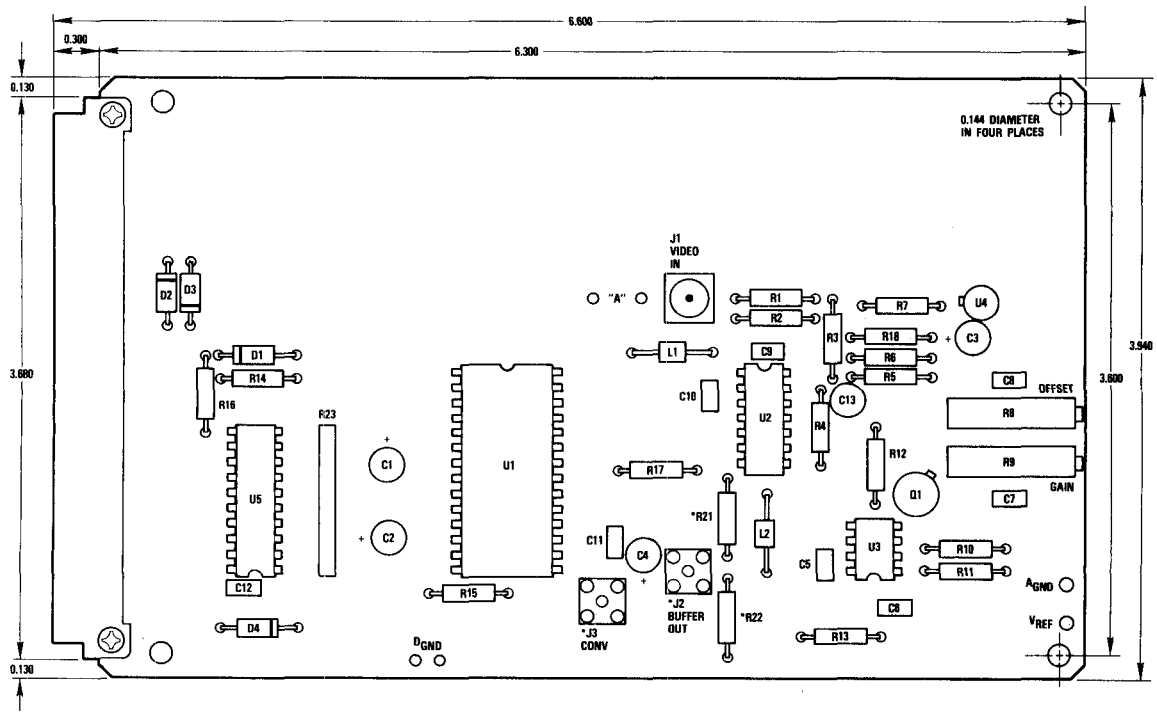
$$R2 = \frac{1}{\frac{VR}{Z_{IN}} + \frac{1}{1000}}$$

and

$$R1 = Z_{IN} - \frac{1000\ R2}{R2 + 1000}$$

where VR is the desired input voltage range of the board, Z_{IN} is the desired input impedance of the board, and the constant value 1000 is given by the value of R3.

Assembly for TDC1048E1C



Note:

1. * not supplied.
2. Dimensions in inches.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
5962-87600 01XC	EXT–T_C = –55°C to 125°C	Per Standard Military Drawing	28 Pin Ceramic DIP	5962-87600 01XC
TDC1048C3C	STD–T_A = 0°C to 70°C	Commercial	28 Contact LCC	1048C3C
TDC1048C3V	EXT–T_C = –55°C to 125°C	MIL-STD-883	28 Contact LCC	1048C3V
5962-87600 013A	EXT–T_C = –55°C to 125°C	Per Standard Military Drawing	28 Contact LCC	5962-87600 013A
TDC1048R3C	STD–T_A = 0°C to 70°C	Commercial	28 Leaded PLCC	1048R3C
TDC1048B6C	STD–T_A = 0°C to 70°C	Commercial	28 Pin CERDIP	1048B6C
TDC1048B6V	EXT–T_C = –55°C to 125°C	MIL-STD-883	28 Pin CERDIP	1048B6V
TDC1048N6C	STD–T_A = 0°C to 70°C	Commercial	28 Pin Plastic DIP	1048N6C
TDC1048E1C	STD–T_A = 0°C to 70°C	– –	Eurocard Format Board with A/D Converter	TDC1048E1C

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