4 MEGA BIT (262,144 WORD × 16 BIT)
CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC574096D is a 262,144 word × 16 bit CMOS ultraviolet light erasable and electrically programmable read only memory. The TC574096D is JEDEC standard pin configuration. This product is packed in 40 pin standard cerdip package.

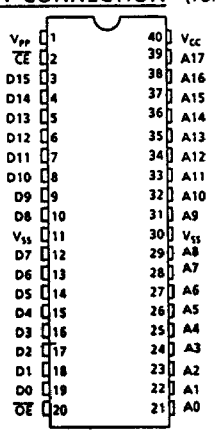
TC574096D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 60mA / 10MHz and access time of 100ns / 120ns.

For progrm operation, the programming is achieved by using the high speed programming mode.

FEATURES

- Peripheral circuit : CMOS
  Memory cell : N-MOS
- Fast access time
  TC574096D-10 : 100ns (V_{CC} = 5.0V ± 5%)
  TC574096D-120 : 120ns (V_{CC} = 5.0V ± 10%)
- Low power dissipation
  Active- : 60mA / 10MHz
  Standby : 100μA
- Single 5V power supply
- Full static operation
- High speed programming operation : t_{PW} 50μs
- Input and output TTL compatible
- JEDEC standard 40 pin
- Standard 40 pin DIP cerdip package

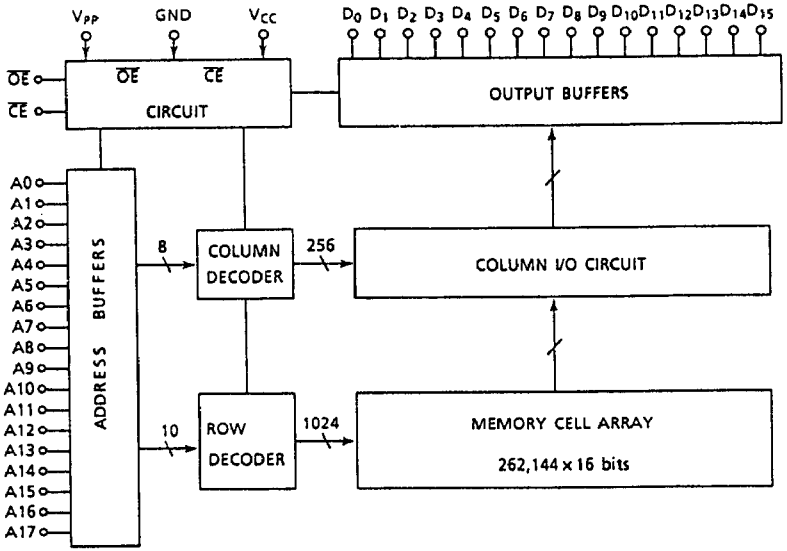
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A17	Address Inputs
D0~D15	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
V_{SS}	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~D15	Power
Read	L	L	5V	5V	Data Out	Active
Output Deselecst	*	H			High Impedance	
Standby	H	*				Standby
Program	L	H	12.50V	6.25V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* : H or L

MAXIMUM RATINGS

SYMBOL	CHARACTERISTIC	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{IN} (A9)	Input Voltage (A9)	−0.6~13.5	V
$V_{I/O}$	Input/Output Voltage	−0.6~V_{CC} + 0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	−65~125	°C
T_{opr}	Operating Temperature	0~70	°C

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	CHARACTERISTIC	TC574096D - 10	TC574096D - 120
Ta	Ambient Temperature	0~70°C	
V_{CC}	V_{CC} Power Supply Voltage	5V ± 5%	5V ± 10%
V_{PP}	V_{PP} Power Supply Voltage	0V~V_{CC} + 0.6V	

DC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	単位
I_{LI}	Input Current	V_{IN} = 0~V_{CC}		-	-	± 10	μA
I_{CCO1}	Operating Current	$\overline{CE}$ = 0V, I_{OUT} = 0mA	f = 8.3MHz	-	-	60	mA
			f = 10MHz	-	-	70	
I_{CCO2}			f = 1MHz	-	-	30	
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$ = V_{CC} - 0.2V		-	-	100	μA
V_{IH}	Input High Voltage	-		2.2	-	V_{CC} + 0	V
V_{IL}	Input Low Voltage	-		- 0.3	-	0.8	V
V_{OH}	Output High Voltage	I_{OH} = - 400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP} = 0V~V_{CC} + 0.6V		-	-	± 10	μA
I_{LO}	Ouptut Leakage Current	V_{OUT} = 0.4V~V_{CC}		-	-	± 10	μA

AC CHARACTERISTICS

SYMBOL	CHARACTERISTIC	TC574096D - 10		TC574096D - 120		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	100	-	120	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	100	-	120	
t_{OE}	$\overline{OE}$ to Output Valid	-	50	-	60	
t_{DF1}	$\overline{CE}$ to Output in High-Z	-	50	-	50	
t_{DF2}	$\overline{OE}$ to Output in High-Z	-	50	-	50	
t_{OH}	Output Data Hold Time	0	-	0	-	

AC TEST CONDITIONS

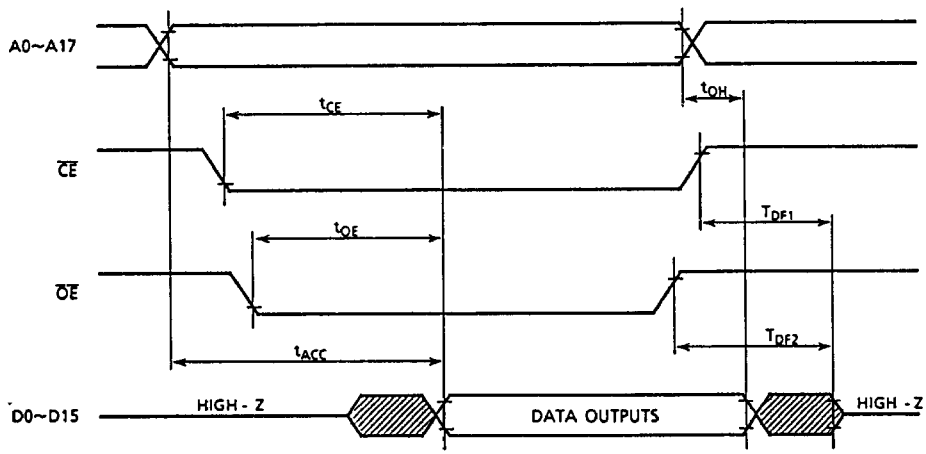
Ouput Load : 1 TTL Gate and C_L=100pF
Input Pulse Rise and Fall Times : 10ns Max.
Input Pulse Levels : 0.45V to 2.4V
Timing Measurement Reference Levels: Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	-	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	-	10	12	

* This characteristic is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.20	12.50	12.80	V

DC AND OPERATING CHARACTERISTICS ($Ta=25\pm5°C, V_{CC}=6.25V\pm0.25V, Vpp=12.50V\pm0.30V$)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	–	–	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=12.8V$	–	–	50	mA

AC PROGRAMMING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6.25V\pm0.25V$, $V_{PP}=12.50V\pm0.30V$)

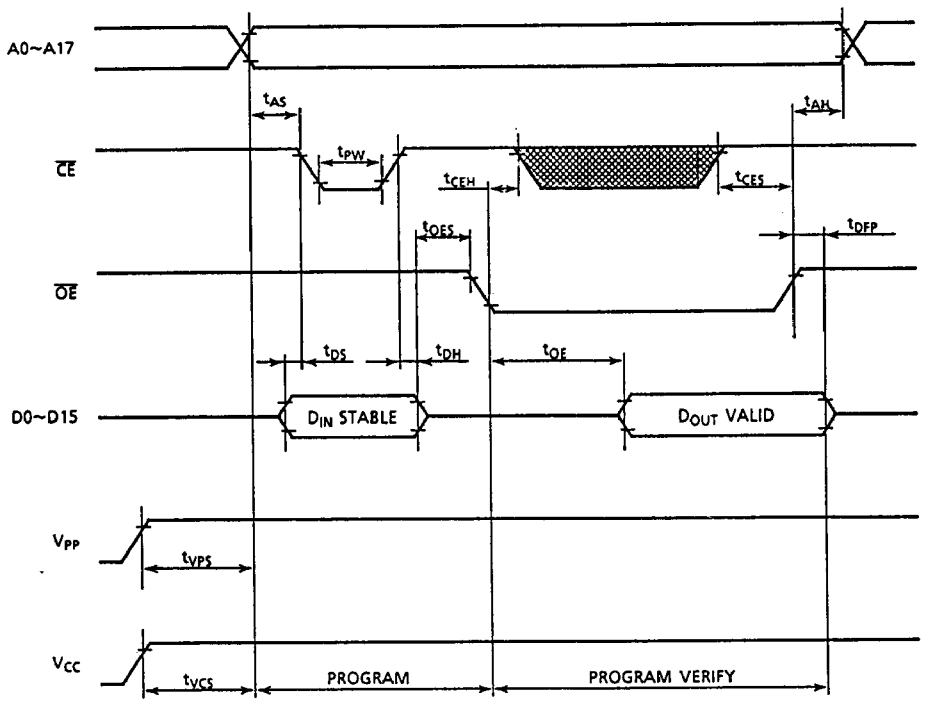
SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	0	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	0	–	–	μs
t_{OES}	$\overline{OE}$ Set up Time	–	2		–	μs
t_{DS}	Data Set up Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VPS}	V_{PP} Set up Time	–	2	–	–	μs
t_{VCS}	V_{CC} Set up Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	–	45	50	55	μs
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	–	–	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	–	–	90	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L=100pF$
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.50V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation.
So the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC574096D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (Ultraviolet light intensity [W/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [W·sec./cm^2].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μW/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW/cm^2] × (20 × 60) [sec] ≃ 15 [W·sec./cm^2].)

The TC574096D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC906 - are available.

OPERATION INFORMATION

The TC574096D's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES		$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~D15	POWER
Read Operation	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*				Standby
Program Operation (Ta = 25 ± 5°C)	Program	L	H	12.50V	6.25V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note : H ; V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TC574096D has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TC574096D's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC574096D has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC574096D is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC574096D are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC574096D is in the programming mode when the V_{PP} input is at 12.50V and $\overline{CE}$ is at Low under $\overline{OE}=V_{IH}$.

The TC574096D can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.50V) is applied to V_{PP} terminal, a high level $\overline{CE}$ and $\overline{OE}$ input inhibits the TC574096D from being programmed.

Programming of two or more TC574096D's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a low level program pulse is applied to the $\overline{CE}$ of the desired device only and high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

The device is set up in the high speed programming mode when the programming voltage (+12.50V) is applied to the V_{PP} terminal with V_{CC}=6.25V.

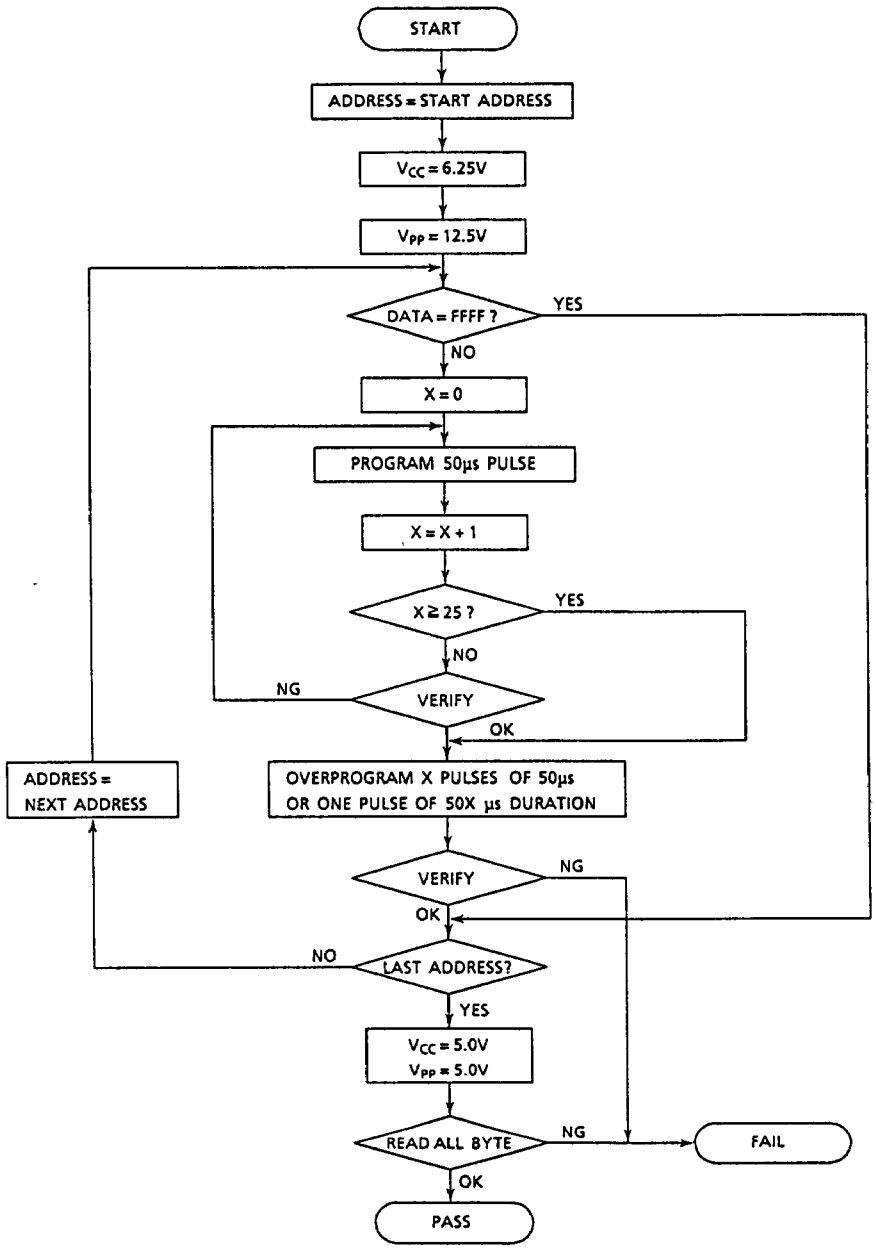
The programming is achieved by applying a single low level 50μs pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 50μs is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 1 time more than that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

HIGH SPEED PROGRAM MODE

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC574096D which identifies it's manufacture and device type.

The programming equipment may read out manufacturer code and device code from TC574096D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC574096D.

PINS / SIGNATURE	A_0	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX DATA
Manufacturer Code	V_{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V_{IH}	*	*	*	*	*	*	*	*	0	0	0	0	1	1	1	0	**0E

Notes : A9 = 12V ± 0.5V,
$A_1 - A_8$, $A_{10} - A_{17}$, $\overline{CE}$, $\overline{OE} = V_{IL}$

*: Don't care

OUTLINE DRAWINGS

• Cerdip DIP

Unit : mm