SED1345

CMOS VIDEO - LCD INTERFACE (VLI)

● **8 Levels of Gray Scale**

■ DESCRIPTION

The SED1345 is a video-LCD interface (VLI) developed for a dot matrix LCD display system. It converts separate video signals for CRT display into signals for LCD.

The SED1345 can use a conventional LCD driver to display data at eight gradation levels corresponding to digital video signal data I, R, G and B. The on-chip color pallet for gradation display allows setting of any gradation level for each of the 16 colors on the CRT display.

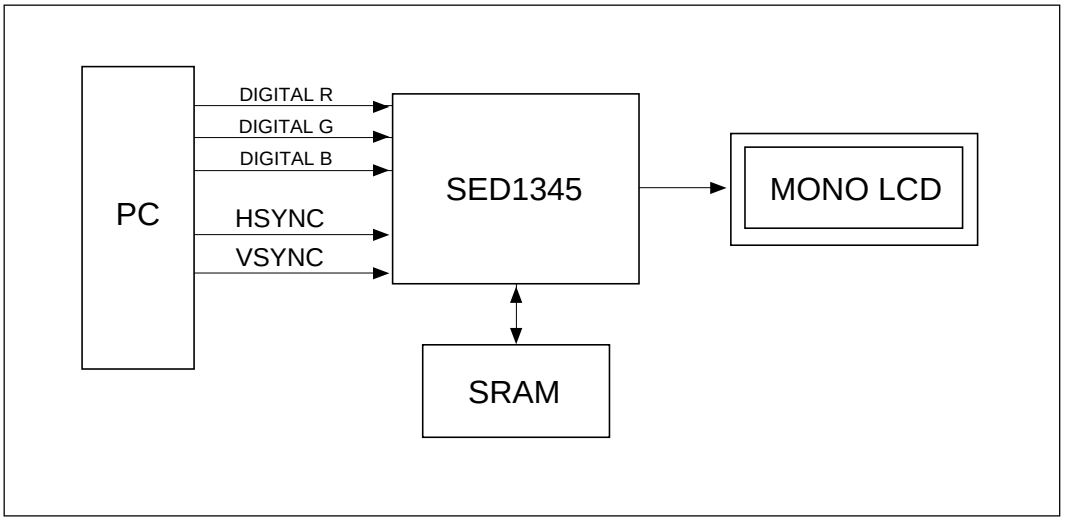
A 640 × 480 dot panel with eight gradation levels can be driven using only 256K bits of frame buffer memory. This leads to a significant reduction in system memory cost.

With the SED1345, the user can select not only a display size but a display area to configure a display panel of flexible size from 640 × 200 dots to 640 × 480 dots (maximum). These LCD display sizes are compatible with various display modes such as CGA® and EGA®.

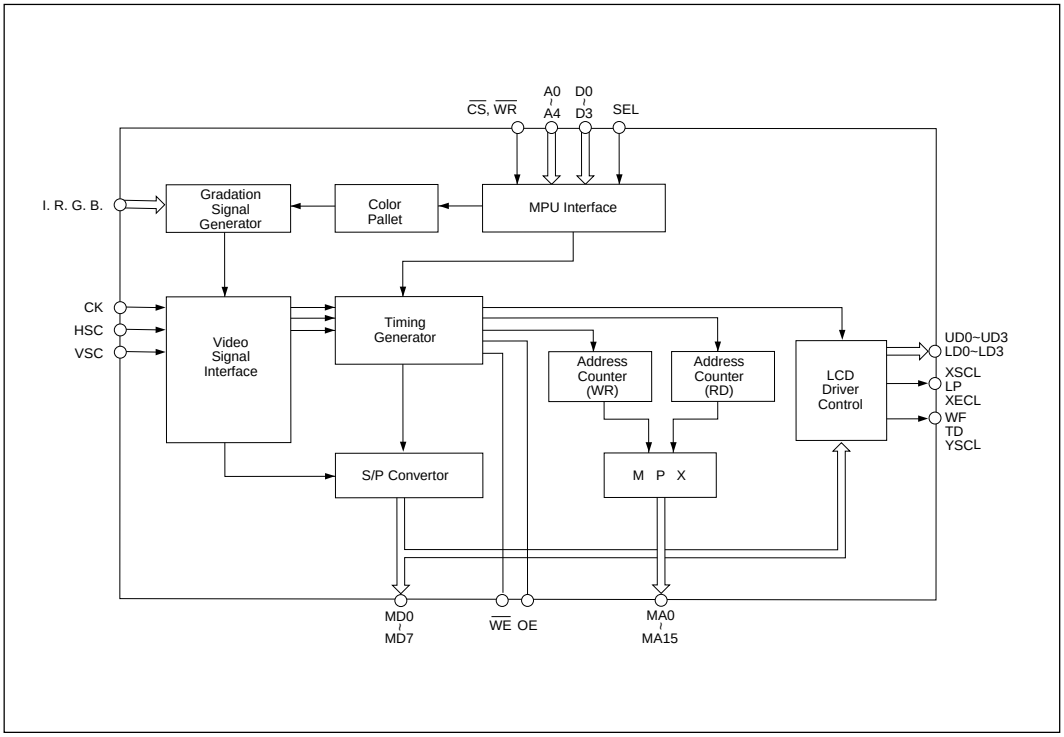
■ FEATURES

- Low-power CMOS technology
- TTL-compatible signal input
- LCD display size:
  Horizontal: ..... 640 dots
  Vertical: ..... 200, 350, 400, 480 lines
- Supports 8 levels of gray shade
- Supports single panel and dual panel
- LCD driver interface:4 bits bus and 4 bits × 2 bus
- Register programming by 4 bits
- Maximum dot clock: ..... 30 MHz
- Supports 40KB SRAM frame buffer
- Duty cycle: ..... 1/200 to 1/480
- Power-on clear function
- Single power supply: ..... 5V ± 5%
- Package: ..... QFP5-80 pin (FOA)

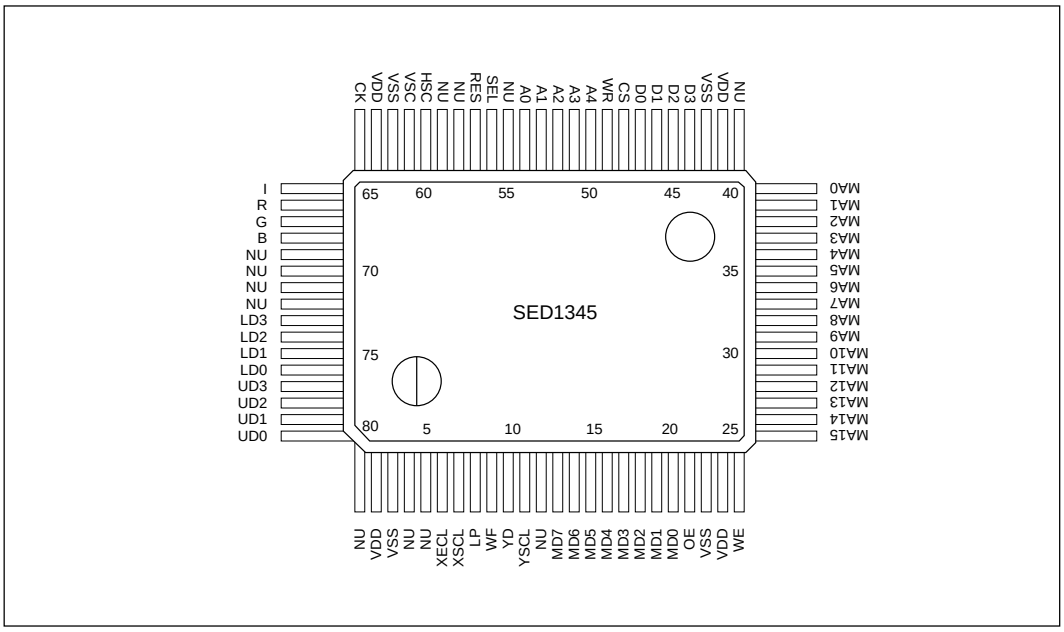
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN OUT



■ PIN OUT

No.	Name	No.	Name	No.	Name	No.	Name
1	NU	21	$\overline{OE}$	41	NU	61	VSC
2	VDD	22	VSS	42	VDD	62	VSS
3	VSS	23	VDD	43	VSS	63	VDD
4	NU	24	$\overline{WE}$	44	D3	64	CK
5	NU	25	MA15	45	D2	65	I
6	XECL	26	MA14	46	D1	66	R
7	XSCL	27	MA13	47	D0	67	G
8	LP	28	MA12	48	$\overline{CS}$	68	B
9	WF	29	MA11	49	$\overline{WR}$	69	NU
10	YD	30	MA10	50	A4	70	NU
11	YSCL	31	MA9	51	A3	71	NU
12	NU	32	MA8	52	A2	72	NU
13	MD7	33	MA7	53	A1	73	LD3
14	MD6	34	MA6	54	A0	74	LD2
15	MD5	35	MA5	55	NU	75	LD1
16	MD4	36	MA4	56	SEL	76	LD0
17	MD3	37	MA3	57	$\overline{RES}$	77	UD3
18	MD2	38	MA2	58	NU	78	UD2
19	MD1	39	MA1	59	NU	79	UD1
20	MD0	40	MA0	60	HSC	80	UD0

Note: NU = Pin is Not Used
The NU pin is wired to the IC chip inside the package, and must be held open.

■ PIN DESCRIPTION

Pin Name	Pin No.	Function
VDD	2, 23, 42, 63	+5V power
VSS	3, 22, 43, 62	GND
UD0 to UD3	80 to 77	Data bus output to X-driver
LD0 to LD3	76 to 73	Data bus output to X-driver
XSCL	7	Shift clock output to X-driver
LP	8	Latch pulse output
XECL	6	Enable shift clock output to X-driver
WF	9	LCD AC signal output
YD	10	Scanning start data output to Y-driver
YSCL	11	Shift clock output to Y-driver
I, R, G, B	65 to 68	Video data input
CK	64	Dot clock input
HSC	60	Horizontal sync signal input
VSC	61	Vertical sync signal input
MA0 to MA15	40 to 25	Address bus output to frame buffer memory
MD0 to MD7	20 to 13	Data bus input/output to frame buffer memory
$\overline{WE}$	24	Write enable signal output
$\overline{OE}$	21	Output enable signal output
D0 to D3	47 to 44	Data bus input for writing registers
A0 to A4	54 to 50	Address bus input/output for writing registers
$\overline{CS}$	48	Chip select signal input
$\overline{WR}$	49	Write signal input
SEL	56	Register write mode selection input (ROM/MPU)
$\overline{RES}$	57	Reset signal input

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition	Ratings	Unit
Supply Voltage	V_{DD}	Based on V_{SS}	–0.3 to 7.0	V
Input Voltage	V_I		–0.3 to V_{DD}+0.3	V
Output Voltage	V_D		–0.3 to V_{DD}+0.3	V
I/O Voltage	$V_{I/O}$		–0.3 to V_{DD}+0.3	V
Output Current/Pin	I_O		–10 to 10	mA
Power Dissipation	P_D		250	mW
Operating Temperature	T_{opr}		0 to 70	°C
Storage Temperature	T_{stg}		–65 to 150	°C
Soldering Temperature and Time	T_{sol}		260°C, 10s (at lead)	—

● Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		4.75	5.00	5.25	V

● DC Characteristics

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Average Operating Current Consumption	I_{opr}	fck=24MHz	—	—	40	mA
High Voltage Input Voltage 1	V_{IH1}	*1	2.0	—	V_{DD}+0.3	V
Low Level Input Voltage 1	V_{IL1}		–0.3	—	0.8	V
High Level Input Voltage 2	V_{IH2}	*2	4.0	—	V_{DD}+0.3	V
Low Level Input Voltage 2	V_{IL2}		–0.3	—	0.8	V
High Level Input Voltage 3	V_{IH3}	*3	3.0	—	V_{DD}+0.3	V
Low Level Input Voltage 3	V_{IL3}		–3.0	—	0.6	V
High Level Output Voltage	V_{OH}	I_{OH} = –2mA	4.35	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 6mA	—	—	0.4	V
Input Current Leakage	IL_I	V_I = 0V to V_{DD}	–1	—	1	µA
I/O Current Leakage	$IL_{I/O}$	$V_{I/O}$ = 0V to V_{DD}	–1	—	1	µA

*1 Pad: I, R, G, B, CK, HSC, VSC, MD0 to MD7, A0 to A4, $\overline{CS}$, $\overline{WR}$

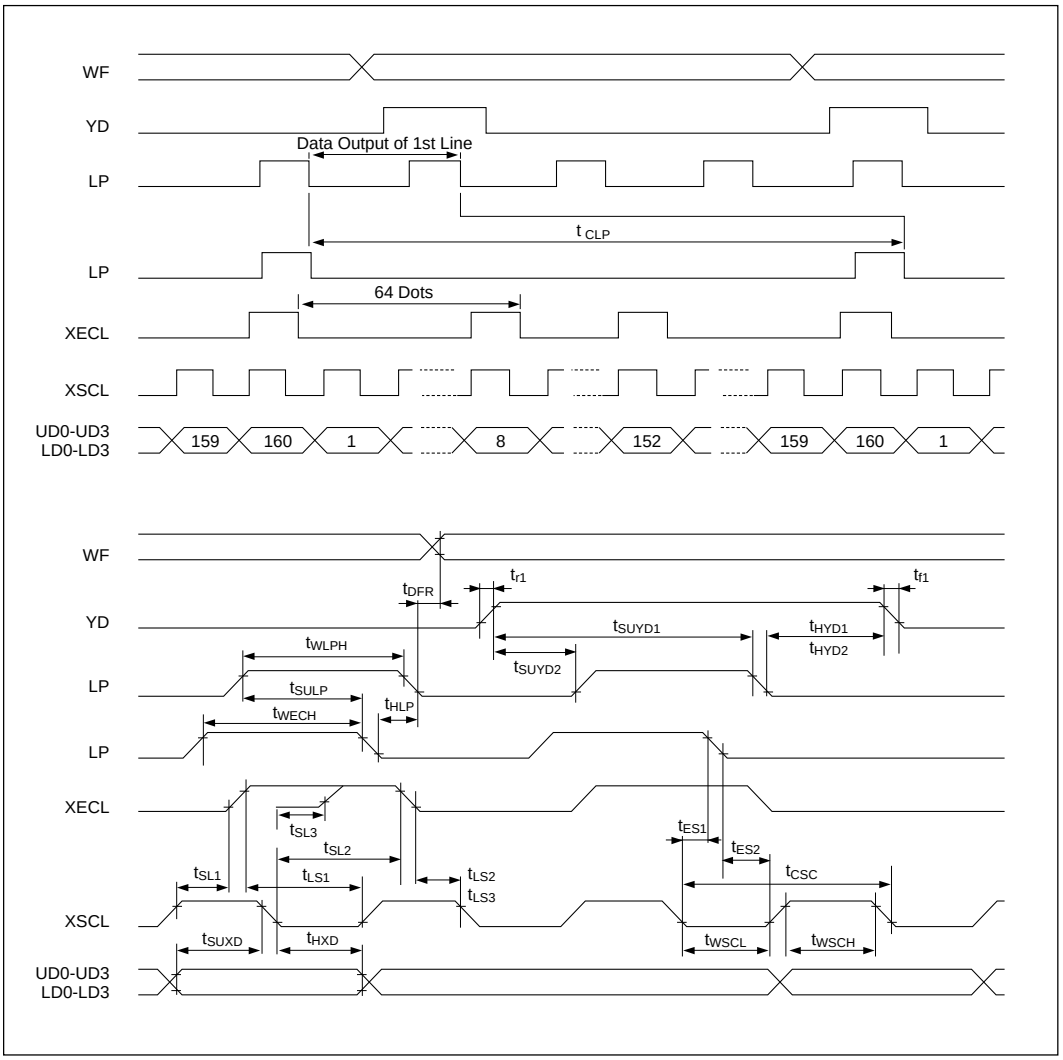
*2 Pad: D0 to D3, SEL

*3 Pad: $\overline{RES}$

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Rise Time	tri	CL = 150pF	—	—	50	ns
Output Fall Time	tfl	CL = 150pF	—	—	50	ns

- **AC CHARACTERISTICS**
  - **LCD Interface Timing Chart**



Output Signal Reference Level: "H" = $V_{DD} \times 0.8V$
"L" = $V_{DD} \times 0.2V$

○ **X Driver**

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
XSCL Cycle Time	t_{CSC}	S6 = "H"		2t1	—	—	ns
		S6 = "L"		4t1			
XSCL "H" Pulse Width	t_{WSCH}	S6 = "H"		t1–20	—	—	ns
		S6 = "L"		2t1–20			
XSCL "L" Pulse Width	t_{WSCL}	S6 = "H"		t1–20	—	—	ns
		S6 = "L"		2t1–20			
UD0–3, LD0–3 Setup Time before XSCL	t_{SUXD}	S6 = "H"		t1–30	—	—	ns
		S6 = "L"		2t1–30			
UD0–3, LD0–3 Hold Time after XSCL	t_{HXD}	S6 = "H"		21–30	—	—	ns
		S6 = "L"		2t1–30			
XSCL to LP Time	t_{SL1}	S5 = "H"	S6 = "H"	0.5t1–30	—	—	ns
			S6 = "L"	t1–30			
XSCL to LP Time	t_{SL2}		S6 = "H"	t1–20	—	—	ns
			S6 = "L"	2t1–20			
LP to XSCL Time	t_{LS1}		S6 = "H"	1.5t1–50	—	—	ns
			S6 = "L"	3t1–50			
LP to XSCL Time	t_{LS2}		S6 = "H"	t1–20	—	—	ns
			S6 = "L"	2t1–20			
XSCL to LP Time	t_{SL3}	S5 = "L"	S6 = "H"	0.5t1–40	—	—	ns
			S6 = "L"	t1–40			
LP to XSCL Time	t_{LS3}		S6 = "H"	0.5t1–40	—	—	ns
			S6 = "L"	t1–40			
LP Cycle Time	t_{CLP}	S0 = "H"		320t1	—	—	ns
		S0 = "L"		640t1			
LP, YSCL "H" Pulse Width	t_{WLPH}	S5 = "H"	S6 = "H"	1.5t1–50	—	—	ns
			S6 = "L"	3t1–50			
		S5 = "L"	S6 = "H"	t1–40	—	—	ns
			S6 = "L"	2t1–40			
LP Setup Time before XECL	t_{SULP}	S5 = "H", S6 = "H"		t1–50	—	—	ns
LP Hold Time after XECL	t_{HLP}	S5 = "H", S6 = "H"		0.5t1–40	—	—	ns
XSCL to XECL Time	t_{ES1}	S5 = "H", S6 = "H"		0.5t1–30	—	—	ns
XECL to XSCL Time	t_{ES2}	S5 = "H", S6 = "H"		0.5t1–40	—	—	ns
XECL "H" Pulse Width	t_{WECH}	S5 = "H", S6 = "H"		1.5t1–50	—	—	ns
WF Output Delay Time After LP, YSCL	t_{DFR}	S5 = "H", S6 = "H"		—	—	100	ns

t1 = 2t_{CCK} (t_{CCK} = dot clock cycle)

○ **Y Driver**

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

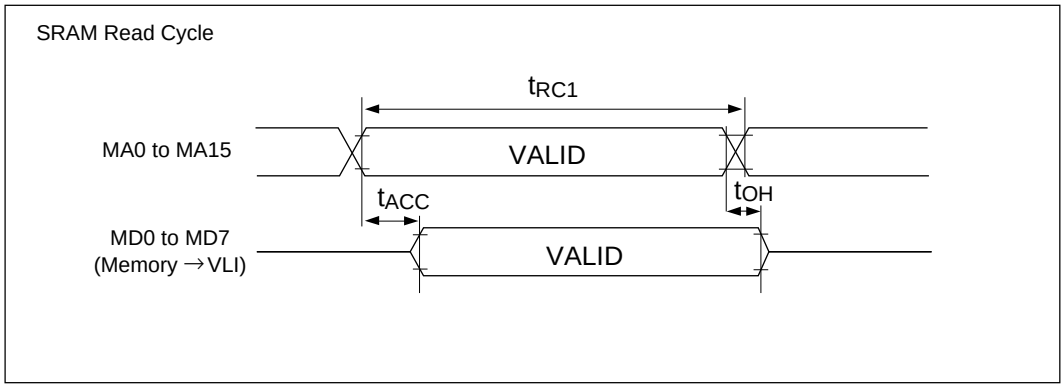
Parameter	Symbol	Condition			Min*	Typ	Max	Unit
YD Setup Time before LP, YSCL	t_{SUYD1}	S5 = "H"	S0 = "H"		142t1–100	—	—	ns
			S0 = "L"		302t1–100			
YD Hold Time after LP, YSCL	t_{hYD1}		S0 = "H"		18t1–100	—	—	ns
			S0 = "L"		18t1–100			
YD Setup Time before LP, YSCL	t_{SUYD2}	S5 = "L"	S0 = "H"	S6 = "H"	141.5t1–100	—	—	ns
				S6 = "L"	141t1–100			
			S0 = "L"	S6 = "H"	301.5t1–100			
				S6 = "L"	301t1–100			
YD Hold Time after LP, YSCL	t_{HYD2}		S0 = "H"	S6 = "H"	17.5t1–100	—	—	ns
				S6 = "L"	17t1–100			
			S0 = "L"	S6 = "H"	17.5t1–100			
				S6 = "L"	17t1–100			

t1=2t_{CCK} (t_{CCK} = dot clock cycle)

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CK Cycle Time	t_{CCK}		33	—	—	ns
CK "H" Pulse Width	t_{WCKW}		12	—	—	ns
CK "L" Pulse Width	t_{WCKL}		12	—	—	ns
Input Rise Time	t_{r2}		—	—	5	ns
Input Fall Time	t_{f2}		—	—	5	ns
VD Setup Time Before CK	t_{SUVD}		16	—	—	ns
VD Hold Time After CK	t_{HVD}		2	—	—	ns
CK Setup Time Before HSC	t_{SUCK}		20	—	—	ns
CK Hold Time After HSC	t_{HCK}		0	—	—	ns
HSC Setup Time Before VSC	t_{SUVH}		80	—	—	ns
HSC Hold Time After VSC	t_{HVM}		0	—	—	ns
Active Pulse Width HSC	t_{WH1}		8t_{CCK}	—	—	ns
Non-Active Pulse Width HSC	t_{WH2}		64t_{CCK}	—	—	ns

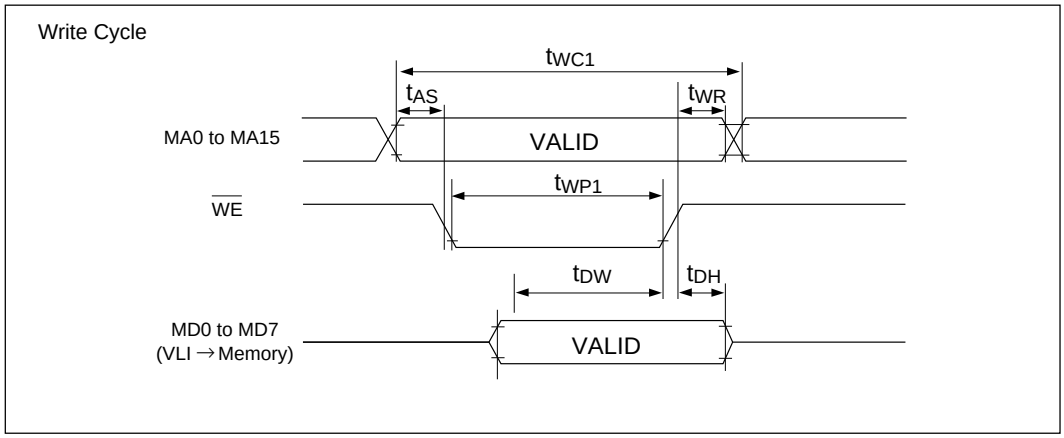
- **Memory Interface**
  - **Read Cycle**



(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Read Cycle Time	t_{RC1}		$4t_{CCK}$	—	—	ns
Address Access Time	t_{ACC}		—	—	$4t_{CCK}$–17	ns
Output Hold Time	t_{OH}		10	—	—	ns

○ **Write Cycle**



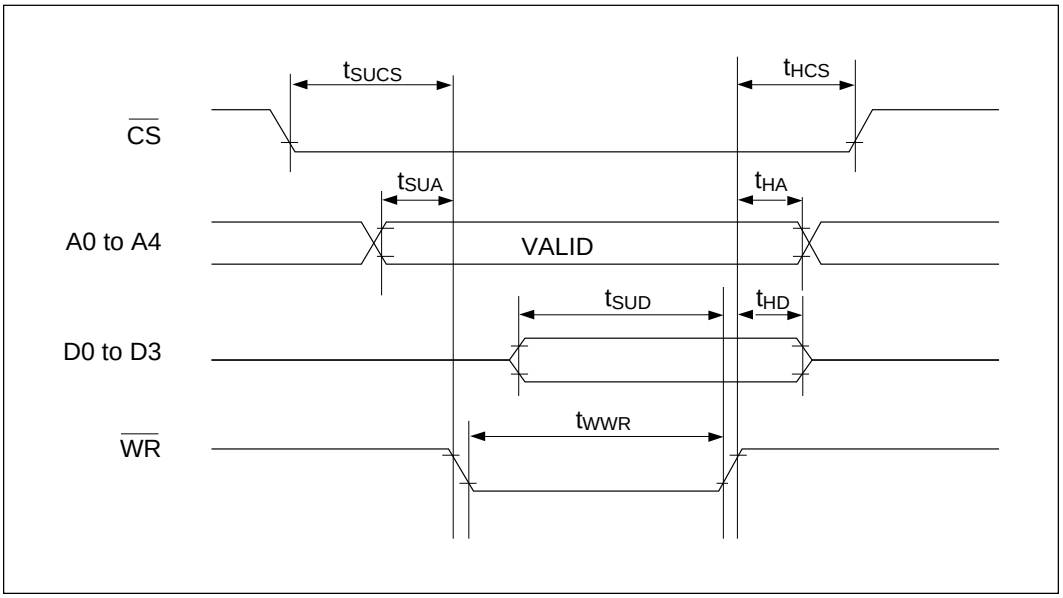
(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min*	Typ	Max	Unit
Write Cycle Time	t_{WC1}		$4t_{CCK}$	—	—	ns
Write Pulse Width	t_{WP1}		$3t_{CCK}$–13	—	—	ns
Address Setup Time	t_{AS}		$0.5t_{CCK}$–14	—	—	ns
Address Hold Time	t_{WR}		$0.5t_{CCK}$–14	—	—	ns
Data Setup Time	t_{DW}		$3t_{CCK}$–38	—	—	ns
Data Hold Time	t_{DH}		5	—	—	ns

Input/Output Signal Reference Level: "H" = 2.0V "L" = 0.8V

*t_{CCK} is the cycle time of dot clock (t_{CCK} = 1/f_{CK}).

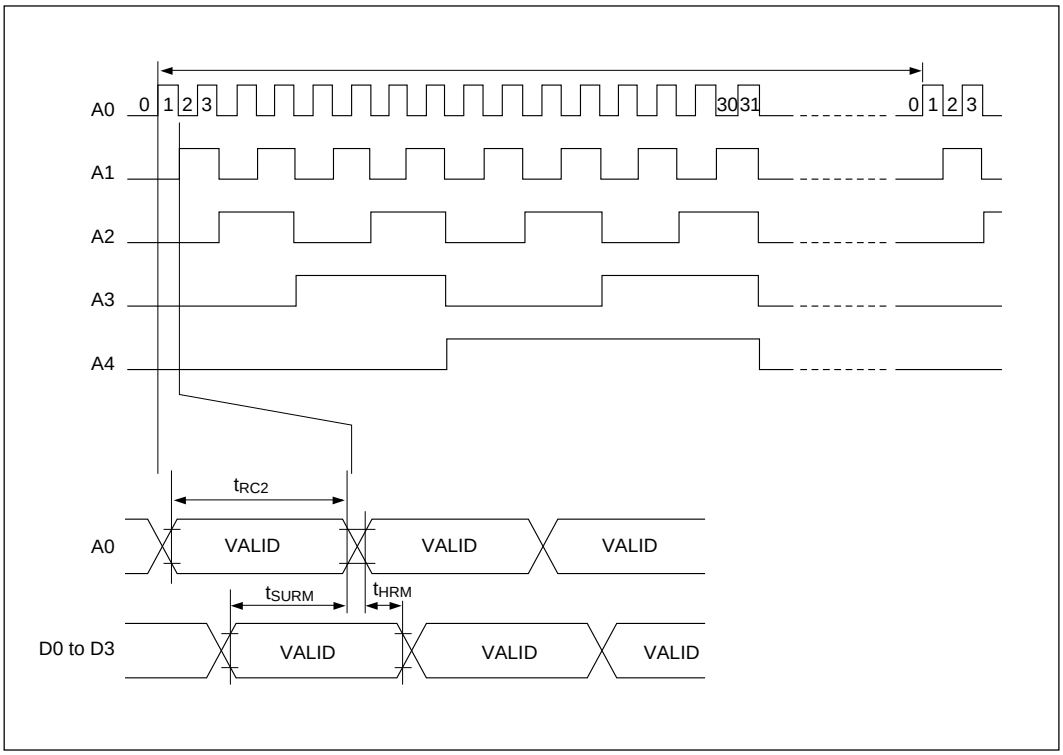
- **Register Program**
  - Write Data Using MPU



(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{CS}$ Setup Time	t_{SUCS}		50	—	—	ns
$\overline{CS}$ Hold Time	t_{HCSH}		50	—	—	ns
A0–A4 Setup Time	t_{SUA}		50	—	—	ns
A0–A4 Hold Time	t_{HA}		50	—	—	ns
D0–D3 Setup Time	t_{SUD}		100	—	—	ns
D0–D3 Hold Time	t_{HD}		50	—	—	ns
$\overline{WR}$ Pulse Width	t_{WWR}		50	—	—	ns

● **Write Data Using ROM**



Input/output signal level identification voltages:

"H" level – 2.0V

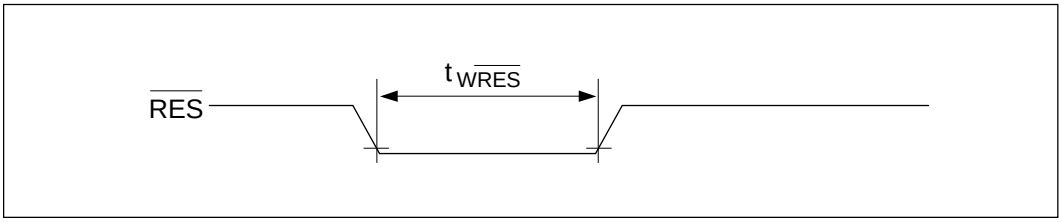
"L" level – 0.8V

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min*	Typ	Max	Unit
ROM Read Cycle Time	t_{RC2}		8t1–100	—	—	ns
D0 to D3 Setup Time	t_{SURM}		100	—	—	ns
D0 to D3 Hold Time	t_{HRM}		10	—	—	ns

* t1=2t_{CCK} (t_{CCK} is a cycle time of dot clock)

- **Reset Input**



(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{RES}$ Pulse Width	tw$\overline{RES}$		1.0	—	—	ns

Input signal reference level: "H" = 2.0V "L" = 0.8V

t_{CCK} is a cycle time of dot clock (t_{CCK} = 1/f_{CK})

- **System Configuration**