N a t i o n a l S e m i c o n d u c t o r

microCMOS

MM82PC08 8-Bit Bidirectional Transceiver

July 1995

General Description

The MM82PC08 is an 8-bit TRI-STATE® high-performance, low-power microCMOS transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured.

One input, Transmit/Receive, determines the direction of logic signals through the bidirectional transceiver; Transmit specifies data flow from Port A to Port B; Receive specifies data flow from Port B to Port A. The Chip Disable input disables both ports by placing them in the TRI-STATE mode.

The MM82PC08 may be utilized in completing NSC800™ high-performance, low-power designs. For military applications, the MM82PC08 is available with class B screening in accordance with Method 5004 of MIL-STD-883.

Features

- microCMOS technology
- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus-oriented systems
- Full interface to CMOS logic levels
- Pinouts simplify system interconnections
- Transmit/receive and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Compact 28-pin leaded chip carrier
- Low power
- Both ports have 150 pF load drive capability
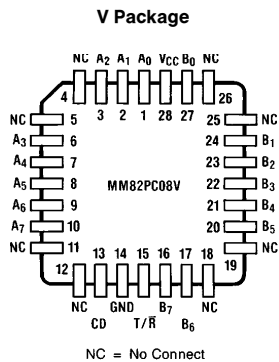- TTL drive capability
  When $V_{CC} = 5V$

System Configuration and Connection Diagrams

TL/C/5595−1

V Package

NC = No Connect

TL/C/5595−6

Dual-In-Line Package
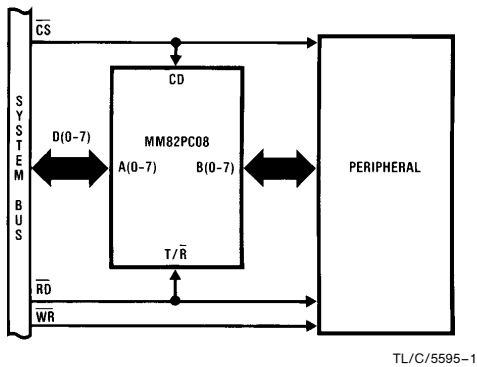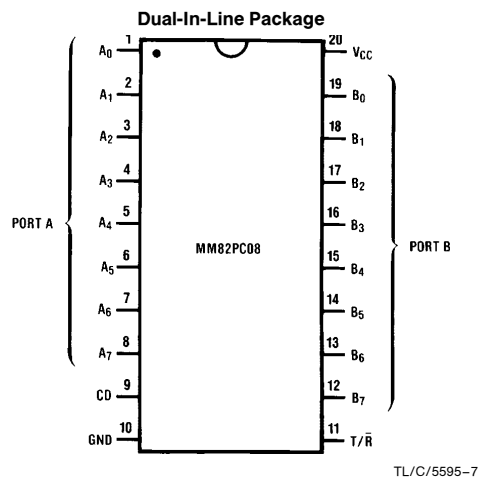
TL/C/5595−7

Top View

Order Number MM82PC08J or N
See NS Package J20A or N20A

Order Number MM82PC08V
See NS Package V28A

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	$-65°C$ to $+150°C$
Voltage at Any Pin with Respect to Ground	$-0.3V$ to $V_{CC} +0.3V$
Lead Temp. (Soldering, 10 seconds)	$300°C$
Power Dissipation	500 mW
Maximum V_{CC}	7V

Note: *Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.*

Operating Conditions $V_{CC} = 5V \pm 10\%$

Ambient Temperature	
Military	$-55°C$ to $+125°C$
Industrial	$-40°C$ to $+85°C$
Commercial	$0°C$ to $+70°C$

DC Electrical Characteristics

$V_{CC} +5V \pm 10\%$, GND $= 0V$, unless otherwise specified

| Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		$0.7 V_{CC}$		V_{CC}	V
V_{IL}	Input Low Voltage		0		$0.2 V_{CC}$	V
V_{OH}	Output High Voltage	$V_{CC} = 4.5V$, $V_{IH} = 4.5V$, $I_{OH} = -2$ mA	2.4			V
V_{OL}	Output Low Voltage	$V_{CC} = 5.5V$, $V_{IL} = 0V$ $V_{IH} = 5.5V$, $I_{OL} = 2$ mA			0.4	V
I_{IH}	Input High Current	$V_{CC} = 5.5V$, $V_{IN} = 5.5V$			10	μA
I_{IL}	Input Low Current	$V_{CC} = 5.5V$, $V_{IN} = 0V$			-10	μA
I_{OH}	Output High Current	$V_{CC} = 4.5V$, $V_{OUT} = 2.4V$, $V_{IH} = 4.5V$	-2.0			mA
I_{OL}	Output Low Current	$V_{CC} = 5.5V$, $V_{OUT} = 0.4V$, $V_{IL} = 0V$	2.0			mA
I_{CC}	Power Supply Current	$V_{CC} = 5.5V$, $V_{IH} = 5.5$,V $V_{IL} = 0V$			400	μA
I_{OZL}	TRI-STATE Low Leakage Current	$V_{CC} = 5.5V$, $V_{OUT} = 0V$			-10	μA
V_{OZH}	TRI-STATE High Leakage Current	$V_{CC} = 4.5V$, $V_{OUT} = 4.5V$			$+10$	μA

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, GND $= 0V$, $C_L = 150$ pF

Symbol	Parameter	Test Conditions	Min	Typ 100 pF	Max 100 pF	Units
t_{DLH}	Propagation Delay to Logical "1" from Port A, B to Port B, A	See *Figure 1*		50	70	ns
t_{DHL}	Propagation Delay to Logical "0" from Port A, B to Port B, A	See *Figure 1*		50	70	ns
t_{ZHTR}	Propagation Delay from High Impedance to Logical "1"from T/R to Port	See *Figure 2*		55	100	ns
t_{ZLTR}	Propagation Delay from High Impedance to Logical "0"from T/R to Port	See *Figure 2*		65	100	ns
t_{HZTR}	Propagation Delay from Logical "1" to High Impedance from T/R to Port	See *Figure 2*		50	100	ns

## AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, GND = 0V, C_L = 150 pF (Continued)

Symbol	Parameter	Test Conditions	Min	Typ 100 pF	Max 100 pF	Units
t_{LZTR}	Propagation Delay from Logical "0" to High Impedance from T/R to Port	See *Figure 2*		55	100	ns
t_{ZH}	Propagation Delay from High Impedance to Logical "1" from CD to Port	See *Figure 3*		50	100	ns
t_{ZL}	Propagation Delay from High Impedance to Logical "0" from CD to Port	See *Figure 3*		65	100	ns
t_{HZ}	Propagation Delay from Logical "1" to High Impedance from CD to Port	See *Figure 3*		50	100	ns
t_{LZ}	Propagation Delay from Logical "0" to High Impedance from CD to Port	See *Figure 3*		55	100	ns

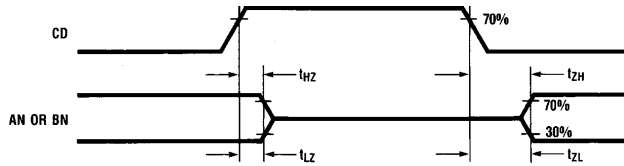## Timing Waveforms
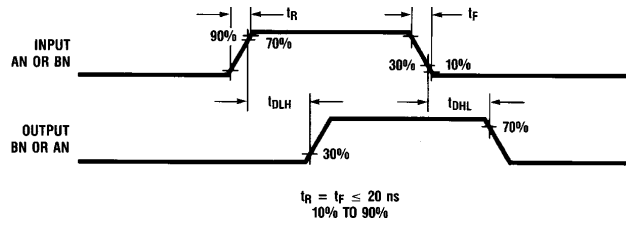
TL/C/5595-2

FIGURE 1. Propagation Delay from Input Port to Output Port
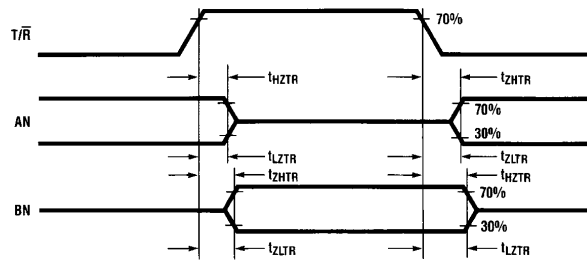
TL/C/5595-3

FIGURE 2. Propagation Delay from T/R to Ports

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Timing Waveforms (Continued)

TL/C/5595-4

FIGURE 3. Propagation Delay from CD to Ports

Pin Descriptions

INPUT SIGNALS

Chip Disable (CD): When CD is high, Port A and Port B are disabled. A low on CD allows data to be transmitted in the direction specified by T/$\overline{R}$.

Transmit/Receive (T/$\overline{R}$): When T/$\overline{R}$ is high, Port A is designated as "IN" and Port B is designated as "OUT." When T/$\overline{R}$ is low, the flow is reversed so that the Port B is "IN" and Port A is "OUT".

INPUT/OUTPUT SIGNALS

Port A (A_0–A_7): Port A is an 8-bit bidirectional port with TRI-STATE outputs for bus-oriented microprocessor and digital communications systems.

Port B (B_0–B_7): Port B is identical to Port A including drive capability.
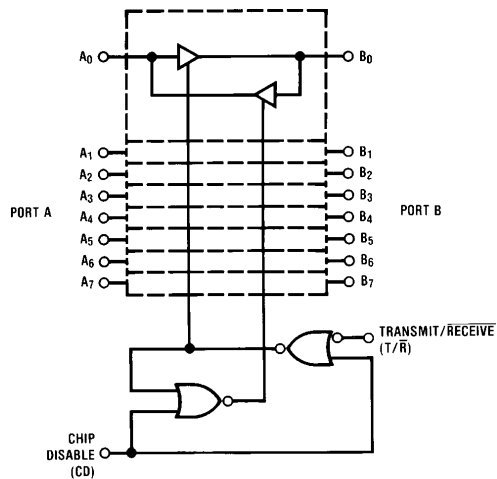
Logic Diagram

TL/C/5595-5

FIGURE 4

Truth Table

Inputs		Resulting Conditions	
Chip Disable	Transmit/$\overline{\text{Receive}}$	Port A	Port B
0	0	OUT	IN
0	1	IN	OUT
1	X	High Z	High Z

X = don't care

Reliability Information

Gate Count 70
Transistor Count 174

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Ordering Information

MM82PC08XXX

/A+ = A+ Reliability Screening
/883 = MIL-STD-883B Screening (Note 1)

I = Industrial Temperature (–40°C to +85°C)
M = Military Temperature (–55°C to +125°C)
No Designation = Commercial Temperature (0°C to +70°C)

N = Plastic Package
J = Cerdip Package
V = Plastic Leaded Chip Carrier (PCC) (Availability to be announced)

TL/C/5595–8

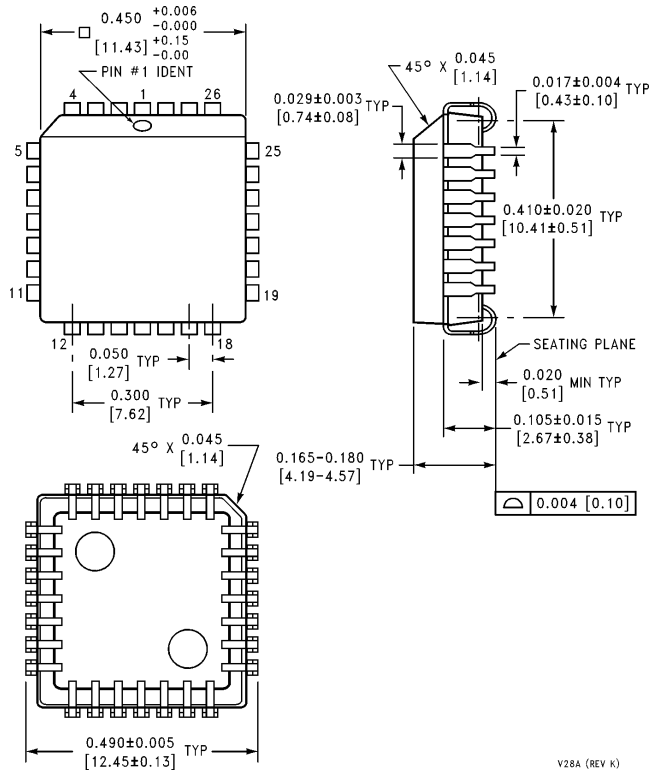**Note 1:** Do not specify a temperature option; all parts are screened to military temperature.

Physical Dimensions inches (millimeters)
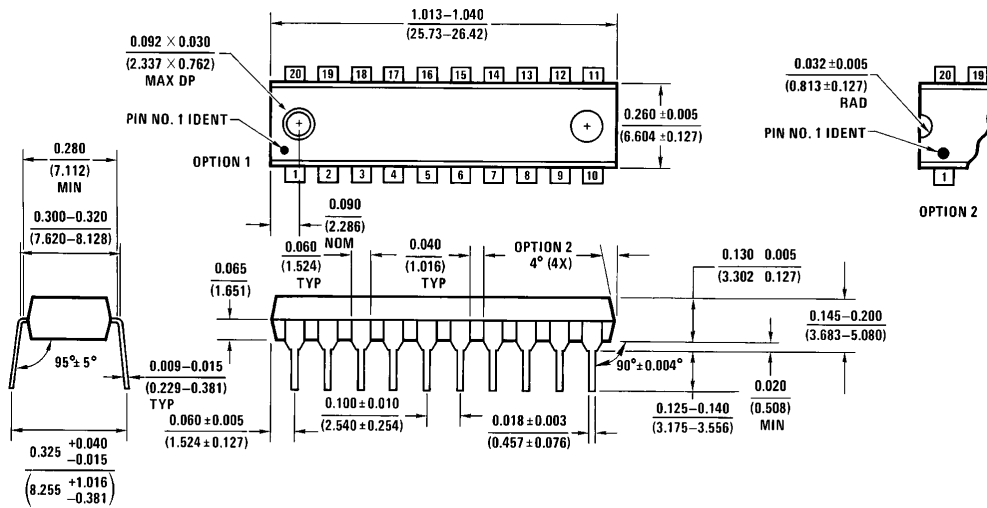
N20A (REV G)

Molded Dual-In-Line Package (N)
Order Number MM82PC08N
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)

0.450 +0.006/−0.000
[11.43] +0.15/−0.00

□ PIN #1 IDENT

0.029±0.003 TYP
[0.74±0.08]

4 1 26

5 25

11 19

12 18

0.050 TYP
[1.27]

0.300 TYP
[7.62]

45° X 0.045
[1.14]

0.490±0.005 TYP
[12.45±0.13]

45° X 0.045
[1.14]

0.017±0.004 TYP
[0.43±0.10]

0.410±0.020 TYP
[10.41±0.51]

SEATING PLANE

0.020 MIN TYP
[0.51]

0.105±0.015 TYP
[2.67±0.38]

0.165−0.180 TYP
[4.19−4.57]

0.004 [0.10]

V28A (REV K)

Plastic Chip Carrier (V)
Order Number MM82PC08V
NS Package Number V28A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.