

MM54HCT03/MM74HCT03 Quad 2-Input NAND Gate (Open Drain)

General Description

The MM54HCT03/MM74HCT03 are logic functions fabricated by using advanced silicon-gate CMOS technology which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are input and output characteristic and pinout compatible with standard DM54LS/74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

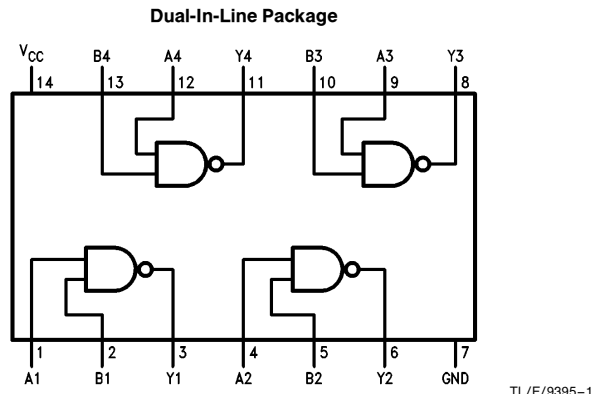
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS

devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

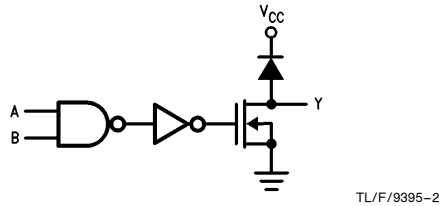
Features

- TTL, LS pin-out and threshold compatible
- Fast switching: $t_{PLH}, t_{PHL} = 12$ ns (typ)
- Low power: 10 μ W at DC
- High fan-out, 10 LS-TTL loads

Connection and Logic Diagrams



Order Number MM54HCT03 or MM74HCT03



Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Voltage (V_{IN})	-1.5V to V_{CC} + 1.5V
DC Output Voltage (V_{OUT})	-0.5V to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	-40	+85	°C
MM54HCT	-55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$			Units	
			Typ	74HCT $T_A = -40^\circ\text{C to } +85^\circ\text{C}$	54HCT $T_A = -55^\circ\text{C to } +125^\circ\text{C}$		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OL}	Maximum Low Level Voltage	$V_{IN} = V_{IH}$		0	0.1	0.1	V
		$ I_{OUT} = 20 \mu\text{A}$	0.2	0.26	0.33	0.4	V
		$ I_{OUT} = 4.0 \text{ mA}, V_{CC} = 4.5\text{V}$	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{LKG}	Minimum High Level Output Leakage Current	$V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = V_{CC}$		0.5	5.0	10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0 \mu\text{A}$		2.0	20	40	μA
		$V_{IN} = 2.4\text{V}$ or 0.5V (Note 4)		1.2	1.4	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package; -12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics $V_{CC} = 5.0V$, $T_A = 25^\circ C$, $C_L = 15 pF$, $t_r = t_f = 6 ns$, unless otherwise noted

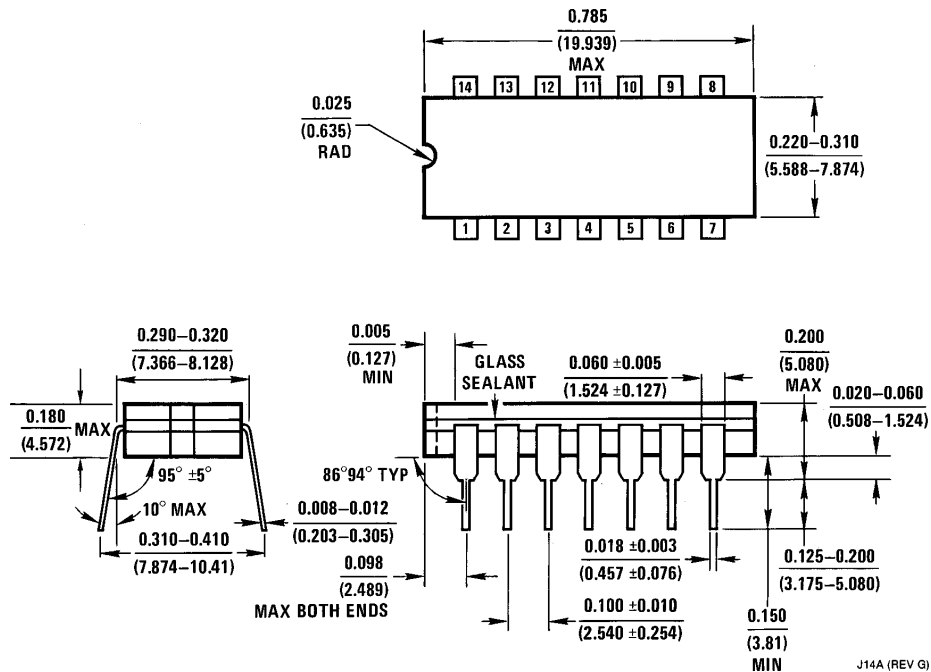
Symbol	Parameter	Conditions	Typ	Units
t_{PZL}	Maximum Propagation Delay	$R_L = 1 k\Omega$	7	ns
t_{PLZ}	Maximum Propagation Delay	$R_L = 1 k\Omega$	10	ns

AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%$, $C_L = 50 pF$, $t_r = t_f = 6 ns$, unless otherwise specified

Symbol	Parameter	Conditions	$T_A \leq 25^\circ$		74HCT	54HCT	Units
			Typ	20	$T_A = -40^\circ C \text{ to } +85^\circ C$	$T_A = -55^\circ C \text{ to } +125^\circ C$	
t_{PZL}	Maximum Propagation Delay	$R_L = 1 k\Omega$	10	20	25	30	ns
t_{PLZ}	Maximum Propagation Delay	$R_L = 1 k\Omega$	12	20	25	30	ns
t_{THL}	Maximum Output Fall Time		10	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate) $R_L = \infty$		14			pF
C_{IN}	Maximum Input Capacitance			5	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

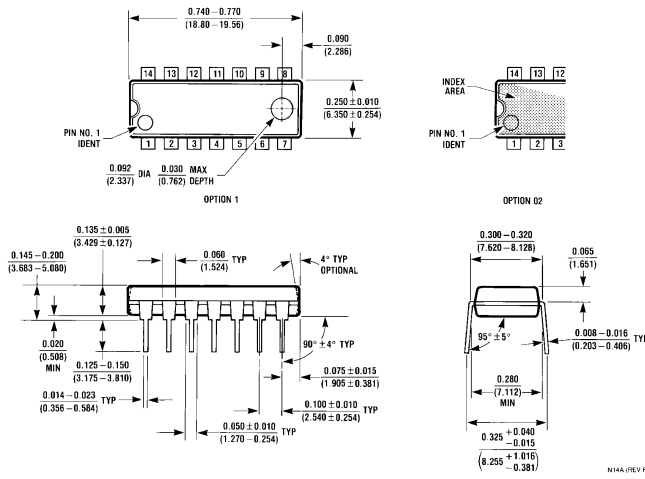
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54HCT03J or MM74HCT03J
NS Package Number J14A

J14A (REV G)

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number MM74HCT03N
NS Package Number N14A

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