- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **pnp Inputs Reduce dc Loading**
- **Data Flowthrough Pinout (All Inputs on Opposite Side From Outputs)**

description

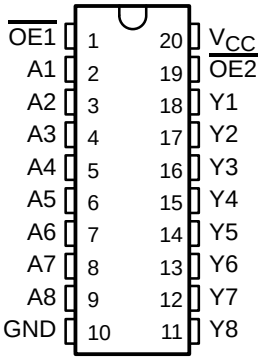
These octal buffers and line drivers are designed to have the performance of the popular SN54ALS240A/SN74ALS240A series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly facilitates printed circuit board layout.

The 3-state control gate is a 2-input NOR gate such that, if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

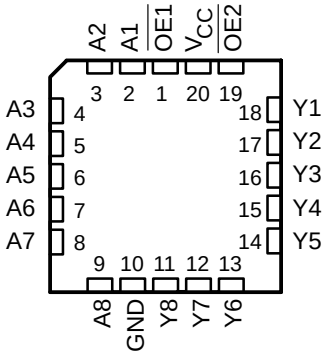
The SN74ALS540 provides inverted data. The 'ALS541 provide true data at the outputs.

The -1 versions of SN74ALS540 and SN74ALS541 are identical to the standard versions, except that the recommended maximum I_{OL} is increased to 48 mA. There is no -1 version of the SN54ALS541.

SN54ALS541 . . . J PACKAGE
SN74ALS540 . . . DW, N, OR NS PACKAGE
SN74ALS541 . . . DB, DW, N, OR NS PACKAGE
(TOP VIEW)



SN54ALS541 . . . FK PACKAGE
(TOP VIEW)



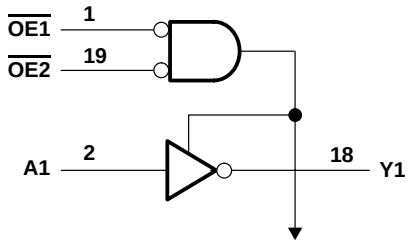
ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS540N	SN74ALS540N
			SN74ALS540-1N	SN74ALS540-1N
			SN74ALS541N	SN74ALS541N
			SN74ALS541-1N	SN74ALS541-1N
	SOIC – DW	Tube	SN74ALS540DW	ALS540
		Tape and reel	SN74ALS540DWR	
		Tube	SN74ALS540-1DW	ALS540-1
		Tube	SN74ALS541DW	ALS541
		Tape and reel	SN74ALS541DWR	
		Tube	SN74ALS541-1DW	ALS541-1
		Tape and reel	SN74ALS541-1DWR	
	SOP – NS	Tape and reel	SN74ALS540NSR	ALS540
		Tape and reel	SN74ALS540-1NSR	ALS540-1
			SN74ALS541NSR	ALS541
			SN74ALS541-1NSR	ALS541-1
	SSOP – DB	Tape and reel	SN74ALS541DBR	G541
			SN74ALS541-1DBR	G541-1
–55°C to 125°C	CDIP – J	Tube	SNJ54ALS541J	SNJ54ALS541J
	LCCC – FK	Tube	SNJ54ALS541FK	SNJ54ALS541FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

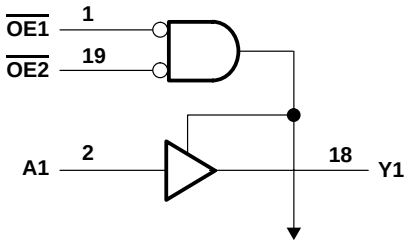
logic diagrams (positive logic)

SN74ALS540



To Seven Other Channels

′ALS541



To Seven Other Channels

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Package thermal impedance, θ_{JA} (see Note 1): DB package . . . . . 70°C/W
DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54ALS541			SN74ALS540 SN74ALS541			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	–55		125	0		70	°C

† Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS541			SN74ALS540 SN74ALS541			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC} –2			V_{CC} –2			V
		V_{CC} = 4.5 V	I_{OH} = –3 mA	2.4	3.2		2.4	3.2		
			I_{OH} = –12 mA	2						
			I_{OH} = –15 mA				2			
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
			I_{OL} = 48 mA†					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			–20			–20	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			–0.2			–0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	–20		–112	–30		–112	mA
I_{CC}	SN74ALS540	V_{CC} = 5.5 V	Outputs high					5	10	mA
			Outputs low					13	22	
			Outputs disabled					11	19	
	'ALS541	V_{CC} = 5.5 V	Outputs high		6	14		6	14	
			Outputs low		15	25		15	25	
			Outputs disabled		13.5	32		13.5	22	

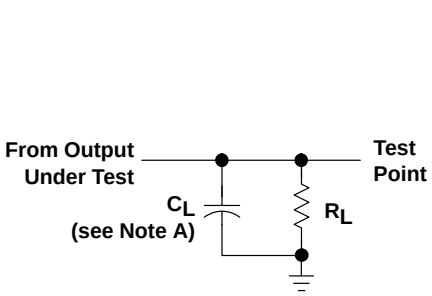
† Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

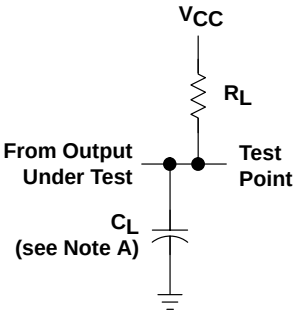
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX¶						UNIT
			SN54ALS541		SN74ALS540		SN74ALS541		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	4	17	2	12	4	14	ns
t_{PHL}			2	14	2	9	2	10	
t_{PZH}	$\overline{OE}$	Y	5	18	5	15	5	15	ns
t_{PZL}			8	28	8	20	8	20	
t_{PHZ}	$\overline{OE}$	Y	1	12	1	10	1	10	ns
t_{PLZ}			2	14	2	12	2	12	

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

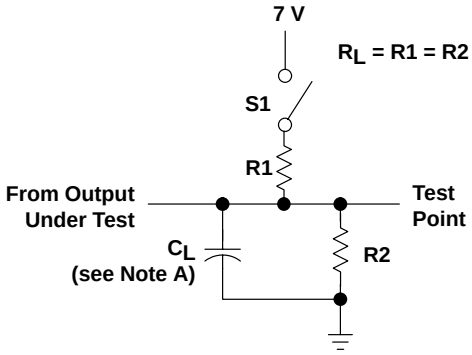
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



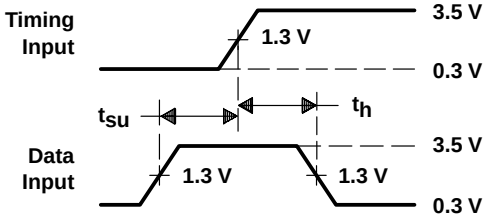
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



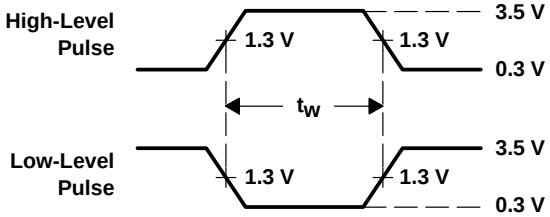
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



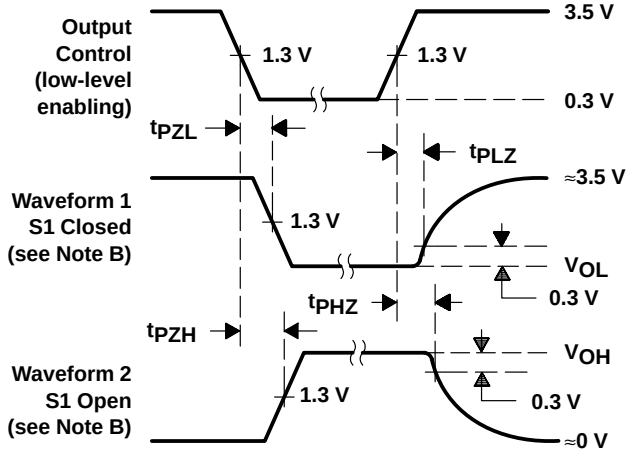
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



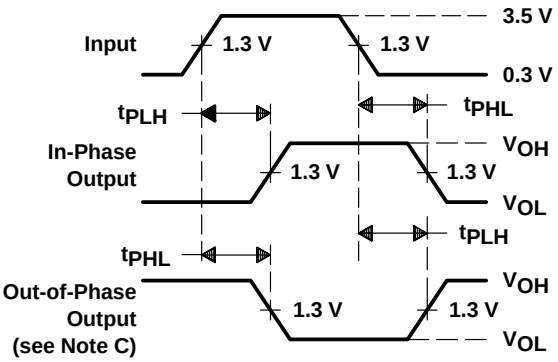
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-89602012A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8960201RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-8960201SA	OBSOLETE	CFP	W	20		None	Call TI	Call TI
SN54ALS541J	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
SN74ALS540-1DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS540-1DWR	OBSOLETE	SOIC	DW	20		None	Call TI	Call TI
SN74ALS540-1N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS540-1NSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS540DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS540DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS540N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS540N3	OBSOLETE	PDIP	N	20		None	Call TI	Call TI
SN74ALS540NSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS541-1DBR	ACTIVE	SSOP	DB	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS541-1DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS541-1DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS541-1N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS541-1NSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS541DBR	ACTIVE	SSOP	DB	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS541DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS541DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS541N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS541N3	OBSOLETE	PDIP	N	20		None	Call TI	Call TI
SN74ALS541NSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ54ALS541FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54ALS541J	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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