MC68HC912BD32/D

MC68HC912BD32

Advance Information

Rev 1.0

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General Description

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Introduction

The MC68HC912BD32 microcontroller unit (MCU) is a16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (CPU12), 32K byte flash EEPROM, 1K byte RAM, 768 byte EEPROM, an asynchronous serial communications interface (SCI), a serial peripheral interface (SPI), an 8-channel timer and 16-bit pulse accumulator, a 10-bit analog-to-digital converter (ADC), a four-channel pulse-width modulator (PWM), and a Byteflight™ module. System resource mapping, clock generation, interrupt control and bus interfacing are managed by the Lite integration module (LIM). The MC68HC912BD32 has full 16-bit data paths throughout, however, the multiplexed external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems.

Features

- 16-Bit CPU12
  - Upward Compatible with M68HC11 Instruction Set
  - Interrupt Stacking and Programmer's Model Identical to M68HC11
  - 20-Bit ALU
  - Instruction Queue
  - Enhanced Indexed Addressing
  - Fuzzy Logic Instructions
- Multiplexed Bus
  - Single Chip or Expanded
  - 16/16 Wide or 16/8 Narrow Modes
- Memory
  - 32K byte Flash EEPROM with 2K byte Erase-Protected Boot Block
  - 768 byte EEPROM
  - 1K byte RAM with Single-Cycle Access for Aligned or Misaligned Read/Write
- 8-Channel, 10-Bit Analog-to-Digital Converter
- 8-Channel Timer
  - Each Channel Fully Configurable as Either Input Capture or Output Compare
  - Simple PWM Mode
  - Modulo Reset of Timer Counter
- 16-Bit Pulse Accumulator
  - External Event Counting
  - Gated Time Accumulation

- Pulse-Width Modulator
  - 8-Bit, 4-Channel or 16-Bit, 2-Channel
  - Separate Control for Each Pulse Width and Duty Cycle
  - Programmable Center-Aligned or Left-Aligned Outputs
- Serial Interfaces
  - Asynchronous Serial Communications Interface (SCI)
  - Synchronous Serial Peripheral Interface (SPI)
- Byteflight™ Module
  - Modular Architecture
  - Implementation of the BMW Byteflight™ protocol
  - Double buffered receive storage systems
  - 16 Message Buffers in total
  - Programmable Message Buffer Configuration (transmit, receive, FIFO)
  - Receive FIFO for bus monitoring with programmable acceptance filter
  - 10 maskable interrupt sources, generating four CPU interrupt vectors
  - Programmable bus master function
  - Programmable wake-up function
  - Low power sleep mode
  - Separate clock system, synchronization to HC12 bus system
- COP Watchdog Timer, Clock Monitor, and Periodic Interrupt Timer
- Features 80-Pin QFP Package
  - Up to 50 General-Purpose I/O Lines
  - 4.75V–5.25V Operation at 10 MHz
- Single-Wire Background Debug™ Mode (BDM)
- On-Chip Hardware Breakpoints

Ordering Information

The MC68HC912BD32 is packaged in 80-pin quad flat pack (QFP) packaging and is shipped in two-piece sample packs, 84-piece trays, or 420-piece bricks. Operating temperature range and voltage requirements are specified when ordering the MC68HC912BD32 device. Refer to Table 1 for part numbers.

Table 1 MC68HC912BD32 Device Ordering Information

Order Number	Temperature		Voltage	Frequency	Package
	Range	Designator			
MC68HC912BD32FU10	0 to +70 °C		4.75V–5.25V	10 MHz	80-Pin QFP Single Tray 84 Pcs
MC68HC912BD32CFU10	–40 to +85 °C	C			

NOTE: *This part is also available in 2-piece sample packs and 420-piece bricks.*

Evaluation boards, assemblers, compilers, and debuggers are available from Motorola and from third-party suppliers. An up-to-date list of products that support the M68HC12 family of microcontrollers can be found on the World Wide Web at the following URL:

http://www.mcu.motsps.com

Documents to assist in product selection are available from the Motorola Literature Distribution Center or your local Motorola Sales Office:

AMCU Device Selection Guide (SG166/D)

AMCU Software and Development Tool Selector Guide (SG176/D)

MC68HC912BD32 Block Diagram

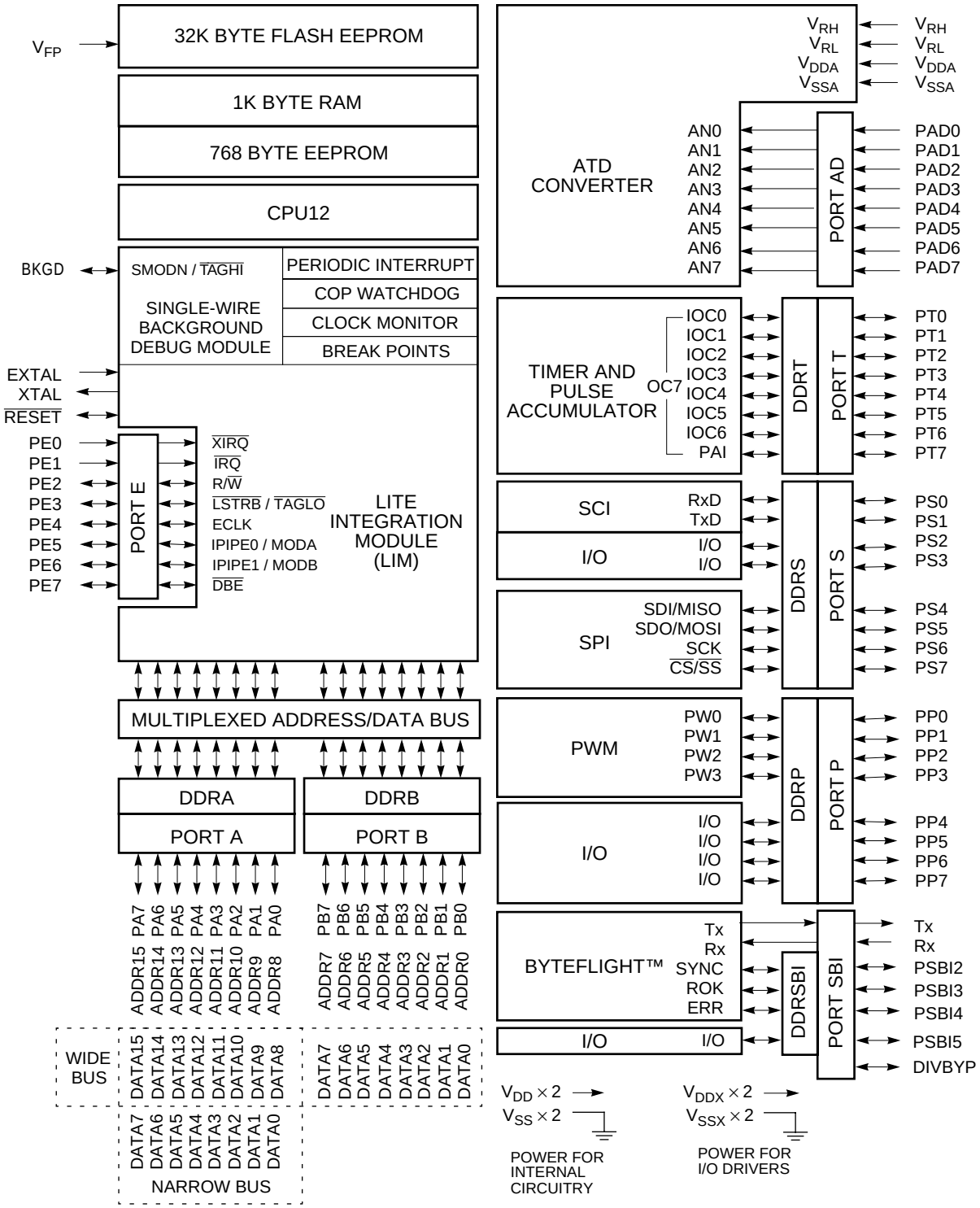

Figure 1 MC68HC912BD32 Block Diagram

General Description

Central Processing Unit

Contents

Introduction

The CPU12 is a high-speed, 16-bit processing unit. It has full 16-bit data paths and wider internal registers (up to 20 bits) for high-speed extended math instructions. The instruction set is a proper superset of the M68HC11instruction set. The CPU12 allows instructions with odd byte counts, including many single-byte instructions. This provides efficient use of ROM space. An instruction queue buffers program information so the CPU always has immediate access to at least three bytes of machine code at the start of every instruction. The CPU12 also offers an extensive set of indexed addressing capabilities.

Programming Model

CPU12 registers are an integral part of the CPU and are not addressed as if they were memory locations.

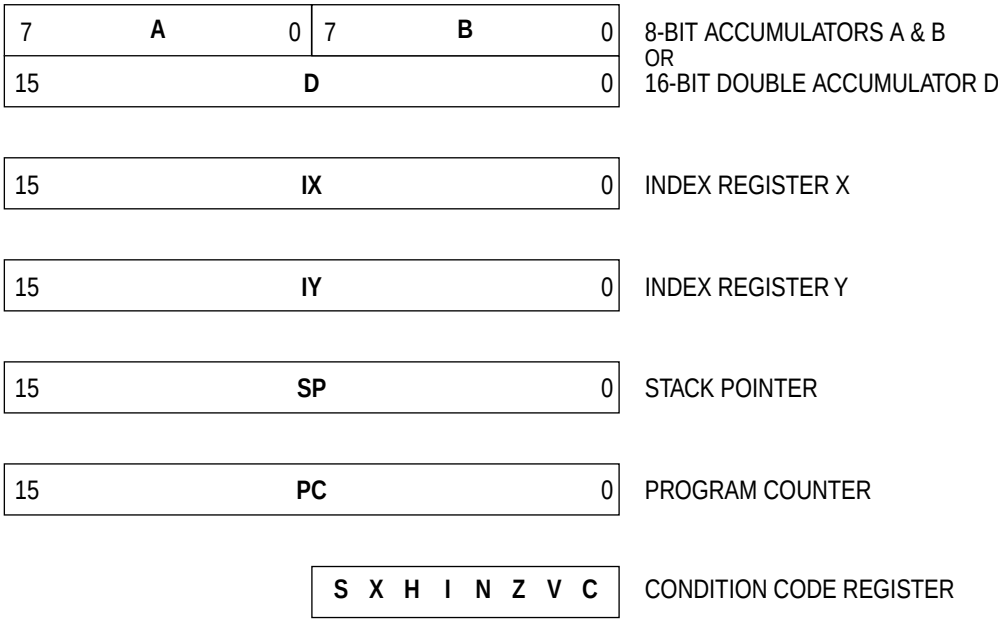

Figure 2 Programming Model

Accumulators A and B are general-purpose 8-bit accumulators used to hold operands and results of arithmetic calculations or data manipulations. Some instructions treat the combination of these two 8-bit accumulators as a 16-bit double accumulator (accumulator D).

Index registers X and Y are used for indexed addressing mode. In the indexed addressing mode, the contents of a 16-bit index register are added to 5-bit, 9-bit, or 16-bit constants or the content of an accumulator to form the effective address of the operand to be used in the instruction.

Stack pointer (SP) points to the last stack location used. The CPU12 supports an automatic program stack that is used to save system context during subroutine calls and interrupts, and can also be used for temporary storage of data. The stack pointer can also be used in all indexed addressing modes.

Program counter is a 16-bit register that holds the address of the next instruction to be executed. The program counter can be used in all indexed addressing modes except autoincrement/decrement.

Condition Code Register (CCR) contains five status indicators, two interrupt masking bits, and a STOP disable bit. The five flags are half carry (H), negative (N), zero (Z), overflow (V), and carry/borrow (C). The half-carry flag is used only for BCD arithmetic operations. The N, Z, V, and C status bits allow for branching based on the results of a previous operation.

After a reset, the CPU fetches a vector from the appropriate address and begins executing instructions. The X and I interrupt mask bits are set to mask any interrupt requests. The S bit is also set to inhibit the STOP instruction.

Data Types

The CPU12 supports the following data types:

- Bit data
- 8-bit and 16-bit signed and unsigned integers
- 16-bit unsigned fractions
- 16-bit addresses

A byte is eight bits wide and can be accessed at any byte location. A word is composed of two consecutive bytes with the most significant byte at the lower value address. There are no special requirements for alignment of instructions or operands.

Addressing Modes

Addressing modes determine how the CPU accesses memory locations to be operated upon. The CPU12 includes all of the addressing modes of the M68HC11 CPU as well as several new forms of indexed addressing. Table 2 is a summary of the available addressing modes.

Table 2 M68HC12 Addressing Mode Summary

Addressing Mode	Source Format	Abbreviation	Description
Inherent	**INST** (no externally supplied operands)	INH	Operands (if any) are in CPU registers
Immediate	**INST** #*opr8i* or **INST** #*opr16i*	IMM	Operand is included in instruction stream 8- or 16-bit size implied by context
Direct	**INST** *opr8a*	DIR	Operand is the lower 8-bits of an address in the range $0000 – $00FF
Extended	**INST** *opr16a*	EXT	Operand is a 16-bit address
Relative	**INST** *rel8* or **INST** *rel16*	REL	An 8-bit or 16-bit relative offset from the current pc is supplied in the instruction
Indexed (5-bit offset)	**INST** *oprx5*,*xysp*	IDX	5-bit signed constant offset from x, y, sp, or pc
Indexed (auto pre-decrement)	**INST** *oprx3*,–*xys*	IDX	Auto pre-decrement x, y, or sp by 1 ~ 8
Indexed (auto pre-increment)	**INST** *oprx3*,+*xys*	IDX	Auto pre-increment x, y, or sp by 1 ~ 8
Indexed (auto post-decrement)	**INST** *oprx3*,*xys*–	IDX	Auto post-decrement x, y, or sp by 1 ~ 8
Indexed (auto post-increment)	**INST** *oprx3*,*xys*+	IDX	Auto post-increment x, y, or sp by 1 ~ 8
Indexed (accumulator offset)	**INST** *abd*,*xysp*	IDX	Indexed with 8-bit (A or B) or 16-bit (D) accumulator offset from x, y, sp, or pc
Indexed (9-bit offset)	**INST** *oprx9*,*xysp*	IDX1	9-bit signed constant offset from x, y, sp, or pc (lower 8-bits of offset in one extension byte)
Indexed (16-bit offset)	**INST** *oprx16*,*xysp*	IDX2	16-bit constant offset from x, y, sp, or pc (16-bit offset in two extension bytes)
Indexed-Indirect (16-bit offset)	**INST [***oprx16*,*xysp***]**	[IDX2]	Pointer to operand is found at... 16-bit constant offset from x, y, sp, or pc (16-bit offset in two extension bytes)
Indexed-Indirect (D accumulator offset)	**INST [D,***xysp***]**	[D,IDX]	Pointer to operand is found at... x, y, sp, or pc plus the value in D

Indexed Addressing Modes

The CPU12 indexed modes reduce execution time and eliminate code size penalties for using the Y index register. CPU12 indexed addressing uses a postbyte plus zero, one, or two extension bytes after the instruction opcode. The postbyte and extensions do the following tasks:

- Specify which index register is used.
- Determine whether a value in an accumulator is used as an offset.
- Enable automatic pre- or post-increment or decrement
- Specify use of 5-bit, 9-bit, or 16-bit signed offsets.

Table 3 Summary of Indexed Operations

Postbyte Code (xb)	Source Code Syntax	Comments
rr0nnnnn	,r n,r –n,r	**5-bit constant offset** n = –16 to +15 rr can specify X, Y, SP, or PC
111rr0zs	n,r –n,r	**Constant offset** (9- or 16-bit signed) z-0 = 9-bit with sign in LSB of postbyte(s) 1 = 16-bit if z = s = 1, 16-bit offset indexed-indirect (see below) rr can specify X, Y, SP, or PC
111rr011	[n,r]	**16-bit offset indexed-indirect** rr can specify X, Y, SP, or PC
rr1pnnnn	n,–r n,+r n,r– n,r+	**Auto pre-decrement/increment** or **Auto post-decrement/increment**; p = pre-(0) or post-(1), n = –8 to –1, +1 to +8 rr can specify X, Y, or SP (PC not a valid choice)
111rr1aa	A,r B,r D,r	**Accumulator offset** (unsigned 8-bit or 16-bit) aa-00 = A 01 = B 10 = D (16-bit) 11 = see accumulator D offset indexed-indirect rr can specify X, Y, SP, or PC
111rr111	[D,r]	**Accumulator D offset indexed-indirect** rr can specify X, Y, SP, or PC

Opcodes and Operands

The CPU12 uses 8-bit opcodes. Each opcode identifies a particular instruction and associated addressing mode to the CPU. Several opcodes are required to provide each instruction with a range of addressing capabilities.

Only 256 opcodes would be available if the range of values were restricted to the number that can be represented by 8-bit binary numbers. To expand the number of opcodes, a second page is added to the opcode map. Opcodes on the second page are preceded by an additional byte with the value $18.

To provide additional addressing flexibility, opcodes can also be followed by a postbyte or extension bytes. Postbytes implement certain forms of indexed addressing, transfers, exchanges, and loop primitives. Extension bytes contain additional program information such as addresses, offsets, and immediate data.

Pinout and Signal Descriptions

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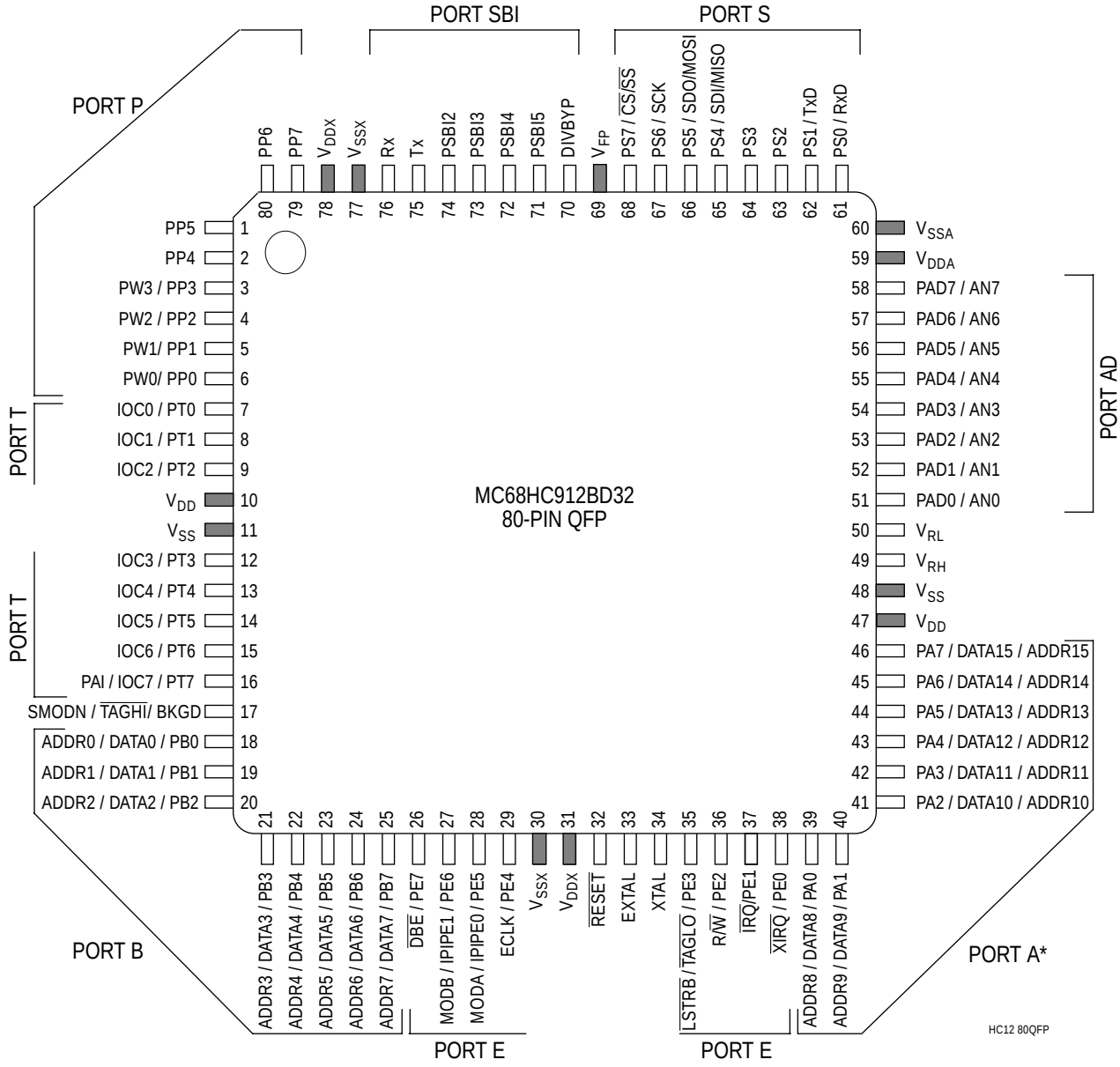
MC68HC912BD32 Rev 1.0 Pin Assignments

The MC68HC912BD32 is available in a 80-pin quad flat pack (QFP). Most pins perform two or more functions, as described in the Signal Descriptions. Figure 3 shows pin assignments. Shaded pins are power and ground.

Pinout and Signal Descriptions



* In narrow mode, high and low data bytes are multiplexed in alternate bus cycles on port A.

Figure 3 Pin Assignments for MC68HC912BD32

Power Supply Pins

MC68HC912BD32 power and ground pins are described below and summarized in Table 4.

Internal Power (V_{DD}) and Ground (V_{SS})

Power is supplied to the MCU through V_{DD} and V_{SS}. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

External Power (V_{DDX}) and Ground (V_{SSX})

External power and ground for I/O drivers. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

V_{DDA}, V_{SSA}

Provides operating voltage and ground for the analog-to-digital converter. This allows the supply voltage to the A/D to be bypassed independently.

Analog to Digital Reference Voltages (V_{RH}, V_{RL})

V_{FP}

Flash EEPROM programming voltage and supply voltage during normal operation.

Table 4 MC68HC912BD32 Power and Ground Connection Summary

Mnemonic	Pin Number	Description
V_{DD}	10, 47	Internal power and ground.
V_{SS}	11, 48	
V_{DDX}	31, 78	External power and ground, supply to pin drivers.
V_{SSX}	30, 77	
V_{DDA}	59	Operating voltage and ground for the analog-to-digital converter, allows the supply voltage to the A/D to be bypassed independently.
V_{SSA}	60	
V_{RH}	49	Reference voltages for the analog-to-digital converter.
V_{RL}	50	
V_{FP}	69	Programming voltage for the Flash EEPROM and required supply for normal operation.

Signal Descriptions

Crystal Driver and External Clock Input (XTAL, EXTAL)

These pins provide the interface for either a crystal or a CMOS compatible clock to control the internal clock generator circuitry. Out of reset the frequency applied to EXTAL is four times the desired E–clock rate (in normal operation with DIVBYP=0; refer to Clock Divider Bypass (DIVBYP)) All the device clocks are derived from the EXTAL input frequency.

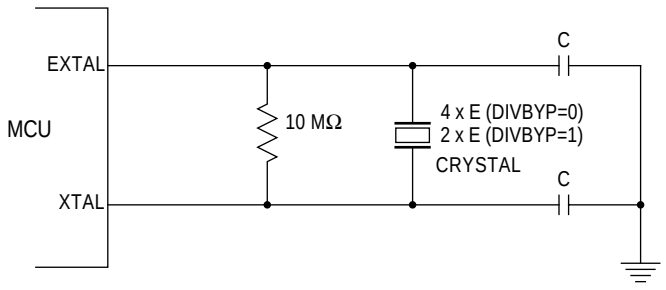


Figure 4 Common Crystal Connections

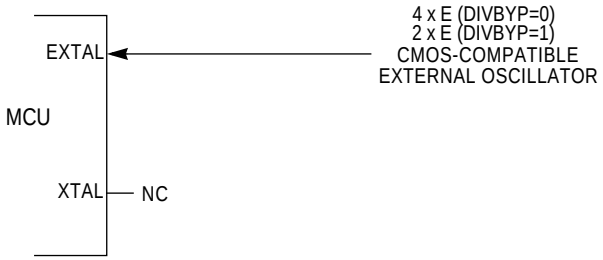


Figure 5 External Oscillator Connections

XTAL is the crystal output.The XTAL pin must be left unterminated when an external CMOS compatible clock input is connected to the EXTAL pin. The XTAL output is normally intended to drive only a crystal. The XTAL output can be buffered with a high-impedance buffer to drive the EXTAL input of another device.

In all cases take extra care in the circuit board layout around the oscillator pins. Load capacitances shown in the oscillator circuits include all stray layout capacitances. Refer to Figure 4 and Figure 5 for diagrams of oscillator circuits.

E-Clock Output (ECLK)

ECLK is the output connection for the internal bus clock and is used to demultiplex the address and data and is used as a timing reference. ECLK frequency is equal to 1/4 the crystal frequency out of reset (in normal operation with DIVBYP=0, refer to Clock Divider Bypass (DIVBYP)).

In normal single-chip mode the E-clock output is off at reset to reduce the effects of RFI, but can be turned on if necessary.

In special single-chip mode the E-clock output is on at reset but can be turned off.

In special peripheral mode the E clock is an input to the MCU.

All clocks, including the E clock, are halted when the MCU is in STOP mode. It is possible to configure the MCU to interface to slow external memory. ECLK can be stretched for such accesses.

Pinout and Signal Descriptions

Reset ($\overline{\text{RESET}}$)

An active low bidirectional control signal, $\overline{\text{RESET}}$, acts as an input to initialize the MCU to a known start-up state. It also acts as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or COP watchdog circuit. The MCU goes into reset asynchronously and comes out of reset synchronously. This allows the part to reach a proper reset state even if the clocks have failed, while allowing synchronized operation when starting out of reset.

It is possible to determine whether a reset was caused by an internal source or an external source. An internal source drives the pin low for 16 cycles; eight cycles later the pin is sampled. If the pin has returned high, either the COP watchdog vector or clock monitor vector will be taken. If the pin is still low, the external reset is determined to be active and the reset vector is taken. Hold reset low for at least 32 cycles to assure that the reset vector is taken in the event that an internal COP watchdog time-out or clock monitor fail occurs.

Maskable Interrupt Request ($\overline{\text{IRQ}}$)

The $\overline{\text{IRQ}}$ input provides a means of applying asynchronous interrupt requests to the MCU. Either falling edge-sensitive triggering or level-sensitive triggering is program selectable (INTCR register). $\overline{\text{IRQ}}$ is always configured to level-sensitive triggering at reset. When the MCU is reset the $\overline{\text{IRQ}}$ function is masked in the condition code register.

This pin is always an input and can always be read. There is an active pull-up on this pin while in reset and immediately out of reset. The pullup can be turned off by clearing PUPE in the PUCR register.

Nonmaskable Interrupt ($\overline{\text{XIRQ}}$)

The $\overline{\text{XIRQ}}$ input provides a means of requesting a nonmaskable interrupt after reset initialization. During reset, the X bit in the condition code register (CCR) is set and any interrupt is masked until MCU software enables it. Because the $\overline{\text{XIRQ}}$ input is level sensitive, it can be connected to a multiple-source wired-OR network. This pin is always an input and can always be read. There is an active pull-up on this pin while in reset and immediately out of reset. The pullup can be turned off by clearing PUPE in the PUCR register. $\overline{\text{XIRQ}}$ is often used as a power loss detect interrupt.

Whenever $\overline{\text{XIRQ}}$ or $\overline{\text{IRQ}}$ are used with multiple interrupt sources ($\overline{\text{IRQ}}$ must be configured for level-sensitive operation if there is more than one source of $\overline{\text{IRQ}}$ interrupt), each source must drive the interrupt input with an open-drain type of driver to avoid contention between outputs. There must also be an interlock mechanism at each interrupt source so that the source holds the interrupt line low until the MCU recognizes and acknowledges the interrupt request. If the interrupt line is held low, the MCU will recognize another interrupt as soon as the interrupt mask bit in the MCU is cleared (normally upon return from an interrupt).

Mode Select (SMODN, MODA, and MODB)

The state of these pins during reset determine the MCU operating mode. After reset, MODA and MODB can be configured as instruction queue tracking signals IPIPE0 and IPIPE1. MODA and MODB have active pulldowns during reset.

The SMODN pin can be used as BKGD or $\overline{\text{TAGHI}}$ after reset.

Single-Wire Background Mode Pin (BKGD)

The BKGD pin receives and transmits serial background debugging commands. A special self-timing protocol is used. The BKGD pin has an active pullup when configured as input; BKGD has no pullup control. Refer to Development Support.

External Address and Data Buses (ADDR[15:0] and DATA[15:0])

External bus pins share function with general-purpose I/O ports A and B. In single-chip operating modes, the pins can be used for I/O; in expanded modes, the pins are used for the external buses.

In expanded wide mode, ports A and B are used for multiplexed 16-bit data and address buses. PA[7:0] correspond to ADDR[15:8]/DATA[15:8]; PB[7:0] correspond to ADDR[7:0]/DATA[7:0].

In expanded narrow mode, ports A and B are used for the16-bit address bus, and an 8-bit data bus is multiplexed with the most significant half of the address bus on port A. In this mode, 16-bit data is handled as two back-to-back bus cycles, one for the high byte followed by one for the low byte. PA[7:0] correspond to ADDR[15:8] and to DATA[15:8] or DATA[7:0], depending on the bus cycle. The state of the address pin

should be latched at the rising edge of E. To allow for maximum address setup time at external devices, a transparent latch should be used.

Read/Write (R/$\overline{W}$)

In all modes this pin can be used as I/O and is a general-purpose input with an active pull-up out of reset. If the read/write function is required it should be enabled by setting the RDWE bit in the PEAR register. External writes will not be possible until enabled.

Low-Byte Strobe ($\overline{LSTRB}$)

In all modes this pin can be used as I/O and is a general-purpose input with an active pull-up out of reset. If the strobe function is required, it should be enabled by setting the LSTRE bit in the PEAR register. This signal is used in write operations and so external low byte writes will not be possible until this function is enabled. This pin is also used as $\overline{TAGLO}$ in Special Expanded modes and is multiplexed with the $\overline{LSTRB}$ function.

Instruction Queue Tracking Signals (IPIPE1 and IPIPE0)

These signals are used to track the state of the internal instruction execution queue. Execution state is time-multiplexed on the two signals. Refer to Development Support.

Data Bus Enable ($\overline{DBE}$)

The $\overline{DBE}$ pin (PE7) is an active low signal that will be asserted low during E-clock high time. $\overline{DBE}$ provides separation between output of a multiplexed address and the input of data. When an external address is stretched, $\overline{DBE}$ is asserted during what would be the last quarter cycle of the last E-clock cycle of stretch. In expanded modes this pin is used to enable the drive control of external buses during external reads. Use of the $\overline{DBE}$ is controlled by the NDBE bit in the PEAR register. $\overline{DBE}$ is enabled out of reset in expanded modes. This pin has an active pullup during and after reset in single chip modes.

Clock Divider Bypass (DIVBYP)

This feature is intended for test purposes only. The DIVBYP pin is input only. The logic state of this static signal is active high. There is an active pull-down on this pin to disable the clock divider bypass when left open. For application it is recommended to tie DIVBYP to VSS. The E-clock rate is 1/4 of the frequency applied to EXTAL.

For test the clock divider bypass is activated by setting DIVBYP to 1. The E-clock rate is 1/2 of the frequency applied to EXTAL.

Table 5 MC68HC912BD32 Signal Description Summary

Pin Name	Pin Number	Description
PW[3:0]	3–6	Pulse Width Modulator channel outputs.
ADDR[7:0] DATA[7:0]	25–18	External bus pins share function with general-purpose I/O ports A and B. In single chip modes, the pins can be used for I/O. In expanded modes, the pins are used for the external buses.
ADDR[15:8] DATA[15:8]	46–39	
IOC[7:0]	16–12, 9–7	Pins used for input capture and output compare in the timer and pulse accumulator subsystem.
PAI	16	Pulse accumulator input
AN[7:0]	58–51	Analog inputs for the analog-to-digital conversion module
DBE	26	Data bus control and, in expanded mode, enables the drive control of external buses during external reads.
MODB, MODA	27, 28	State of mode select pins during reset determine the initial operating mode of the MCU. After reset, MODB and MODA can be configured as instruction queue tracking signals IPIPE1 and IPIPE0 or as general-purpose I/O pins.
IPIPE1, IPIPE0	27, 28	
ECLK	29	E Clock is the output connection for the external bus clock. ECLK is used as a timing reference and for address demultiplexing.
RESET	32	An active low bidirectional control signal, $\overline{\text{RESET}}$ acts as an input to initialize the MCU to a known start-up state, and an output when COP or clock monitor causes a reset.
EXTAL	33	Crystal driver and external clock input pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.
XTAL	34	
LSTRB	35	Low byte strobe (0 = low byte valid), in all modes this pin can be used as I/O. The low strobe function is the exclusive-NOR of A0 and the internal $\overline{\text{SZ8}}$ signal. (The $\overline{\text{SZ8}}$ internal signal indicates the size 16/8 access.)
TAGLO	35	Pin used in instruction tagging. See Development Support.
R/$\overline{\text{W}}$	36	Indicates direction of data on expansion bus. Shares function with general-purpose I/O. Read/write in expanded modes.
IRQ	37	Maskable interrupt request input provides a means of applying asynchronous interrupt requests to the MCU. Either falling edge-sensitive triggering or level-sensitive triggering is program selectable (INTCR register).
XIRQ	38	Provides a means of requesting asynchronous nonmaskable interrupt requests after reset initialization
BKGD	17	Single-wire background interface pin is dedicated to the background debug function. During reset, this pin determines special or normal operating mode.
TAGHI	17	Pin used in instruction tagging. See Development Support.
Rx	76	Byteflight™ receive pin
Tx	75	Byteflight™ transmit pin

Table 5 MC68HC912BD32 Signal Description Summary

Pin Name	Pin Number	Description
$\overline{CS}$/$\overline{SS}$	68	Slave select output for SPI master mode, input for slave mode or master mode.
SCK	67	Serial clock for SPI system.
SDO/MOSI	66	Master out/slave in pin for serial peripheral interface
SDI/MISO	65	Master in/slave out pin for serial peripheral interface
TxD	62	SCI transmit pin
RxD	61	SCI receive pin
DIVBYP	70	Clock divider bypass

Port Signals

The MC68HC912BD32 incorporates eight ports which are used to control and access the various device subsystems. When not used for these purposes, port pins may be used for general-purpose I/O. In addition to the pins described below, each port consists of a data register which can be read and written at any time, and, with the exception of port AD, PE[1:0] and port SBI[1:0], a data direction register which controls the direction of each pin. After reset all port pins are configured as input.

Port A

Port A pins are used for address and data in expanded modes. The port data register is not in the address map during expanded and peripheral mode operation. When it is in the map, port A can be read or written at anytime.

Register DDRA determines whether each port A pin is an input or output. DDRA is not in the address map during expanded and peripheral mode operation. Setting a bit in DDRA makes the corresponding bit in port A an output; clearing a bit in DDRA makes the corresponding bit in port A an input. The default reset state of DDRA is all zeroes.

When the PUPA bit in the PUCR register is set, all port A input pins are pulled-up internally by an active pull-up device. This bit has no effect if the port is being used in expanded modes as the pull-ups are inactive.

Setting the RDPA bit in register RDRIV causes all port A outputs to have reduced drive level. RDRIV can be written once after reset. RDRIV is not

in the address map in peripheral mode. Refer to Bus Control and Input/Output.

Port B

Port B pins are used for address and data in expanded modes. The port data register is not in the address map during expanded and peripheral mode operation. When it is in the map, port B can be read or written at anytime.

Register DDRB determines whether each port B pin is an input or output. DDRB is not in the address map during expanded and peripheral mode operation. Setting a bit in DDRB makes the corresponding bit in port B an output; clearing a bit in DDRB makes the corresponding bit in port B an input. The default reset state of DDRB is all zeroes.

When the PUPB bit in the PUCR register is set, all port B input pins are pulled-up internally by an active pull-up device. This bit has no effect if the port is being used in expanded modes as the pull-ups are inactive.

Setting the RDPB bit in register RDRIV causes all port B outputs to have reduced drive level. RDRIV can be written once after reset. RDRIV is not in the address map in peripheral mode. Refer to Bus Control and Input/Output.

Port E

Port E pins operate differently from port A and B pins. Port E pins are used for bus control signals and interrupt service request signals. When a pin is not used for one of these specific functions, it can be used as general-purpose I/O. However, two of the pins (PE[1:0]) can only be used for input, and the states of these pins can be read in the port data register even when they are used for $\overline{\text{IRQ}}$ and $\overline{\text{XIRQ}}$.

The PEAR register determines pin function, and register DDRE determines whether each pin is an input or output when it is used for general-purpose I/O. PEAR settings override DDRE settings. Because PE[1:0] are input-only pins, only DDRE[7:2] have effect. Setting a bit in the DDRE register makes the corresponding bit in port E an output; clearing a bit in the DDRE register makes the corresponding bit in port E an input. The default reset state of DDRE is all zeroes.

When the PUPE bit in the PUCR register is set, PE[7,3,2,1,0] are pulled up. PE[7,3,2,1,0] are pulled up active devices, while PE1 is always pulled up by means of an internal resistor.

Neither port E nor DDRE is in the map in peripheral mode; neither is in the internal map in expanded modes with EME set.

Setting the RDPE bit in register RDRIV causes all port E outputs to have reduced drive level. RDRIV can be written once after reset. RDRIV is not in the address map in peripheral mode. Refer to Bus Control and Input/Output.

Port SBI

The port SBI has four general-purpose I/O pins, PSBI[5:2]. The DIVBYP pin, the Byteflight™ receive pin, Rx, and transmit pin, Tx, cannot be configured as general-purpose I/O on port SBI.

Register DDRSBI determines whether each port SBI pin PSBI[5:2] is an input or output. Setting a bit in DDRSBI makes the corresponding pin in port SBI an output; clearing a bit makes the corresponding pin an input. After reset port SBI pins PSBI[5:2] are configured as inputs.

When a read to the port SBI is performed, the values for Bit 7 and Bit 6 depend on the contents of the port SBI data register, PORTSBI[7:6] and the of contents of DDRSBI[7:6]. Refer to Table 6 for the returned values.

Table 6 Port SBI Read accesses

DDRSBI[Bit x]	Read data values		
	Bit 7	Bit 6	Bit 5... Bit 2
0	0	DIVBYP	PSBI[5:2]
1	PORTSBI[7]	PORTSBI[6]	PORTSBI[5:2]

When the PUESBI bit in the PCTLSBI register is set, port SBI input pins PSBI[5:2] are pulled up internally by an active pull-up device.

Setting the RDRSBI bit in register PCTLSBI causes the port SBI outputs PSBI[5:2] to have reduced drive level. Levels are at normal drive capability after reset. RDRSBI can be written anytime after reset. Refer to Byteflight™ Module.

Port AD

Input to the analog-to-digital subsystem and general-purpose input. When analog-to-digital functions are not enabled, the port has eight general-purpose input pins, PAD[7:0]. The ADPU bit in the ATDCTL2 register enables the A/D function.

Port AD pins are inputs; no data direction register is associated with this port. The port has no resistive input loads and no reduced drive controls. Refer to Analog to Digital Converter.

Port P

The four pulse-width modulation channel outputs share general-purpose port P pins. The PWM function is enabled with the PWEN register. Enabling PWM pins takes precedence over the general-purpose port. When pulse-width modulation is not in use, the port pins may be used for general-purpose I/O.

Register DDRP determines pin direction of port P when used for general-purpose I/O. When DDRP bits are set, the corresponding pin is configured for output. On reset the DDRP bits are cleared and the corresponding pin is configured for input.

When the PUPP bit in the PWCTL register is set, all input pins are pulled up internally by an active pull-up device. Pullups are disabled after reset.

Setting the RDPP bit in the PWCTL register configures all port P outputs to have reduced drive levels. Levels are at normal drive capability after reset. The PWCTL register can be read or written anytime after reset. Refer to Pulse Width Modulator.

Port T

This port provides eight general-purpose I/O pins when not enabled for input capture and output compare in the timer and pulse accumulator subsystem. The TEN bit in the TSCR register enables the timer function. The pulse accumulator subsystem is enabled with the PAEN bit in the PACTL register.

Register DDRT determines pin direction of port T when used for general-purpose I/O. When DDRT bits are set, the corresponding pin is configured for output. On reset the DDRT bits are cleared and the corresponding pin is configured for input.

When the PUPT bit in the TMSK2 register is set, all input pins are pulled up internally by an active pull-up device. Pullups are disabled after reset.

Setting the RDPT bit in the TMSK2 register configures all port T outputs to have reduced drive levels. Levels are at normal drive capability after reset. The TMSK2 register can be read or written anytime after reset Refer to Standard Timer Module.

Port S

Port S is the 8-bit interface to the standard serial interface consisting of the serial communications interface (SCI) and serial peripheral interface (SPI) subsystems. Port S pins are available for general-purpose parallel I/O when standard serial functions are not enabled.

Port S pins serve several functions depending on the various internal control registers. If WOMS bit in the SC0CR1register is set, the P-channel drivers of the output buffers are disabled for bits 0 through 1 (2 through 3). If SWOM bit in the SP0CR1 register is set, the P-channel drivers of the output buffers are disabled for bits 4 through 7. (wired-OR mode). The open drain control effects to both the serial and the general-purpose outputs. If the RDPSx bits in the PURDS register are set, the appropriate Port S pin drive capabilities are reduced. If PUPSx bits in the PURDS register are set, the appropriate pull-up device is connected to each port S pin which is programmed as a general-purpose input. If the pin is programmed as a general-purpose output, the pull-up is disconnected from the pin regardless of the state of the individual PUPSx bits. See Serial Interface.

Table 7 MC68HC912BD32 Port Description Summary

Port Name	Pin Numbers	Data Direction DD Register (Address)	Description
Port A PA[7:0]	46–39	In/Out DDRA ($0002)	Port A and port B pins are used for **address** and **data** in expanded modes. The port data registers are not in the address map during expanded and peripheral mode operation. When in the map, port A and port B can be read or written any time. DDRA and DDRB are not in the address map in expanded or peripheral modes.
Port B PB[7:0]	25–18	In/Out DDRB ($0003)	
Port AD PAD[7:0]	58–51	In	**Analog-to-digital converter** and general-purpose I/O.

Table 7 MC68HC912BD32 Port Description Summary

Port Name	Pin Numbers	Data Direction DD Register (Address)	Description
Port SBI DIVBYP PSBI[5:2] TxSBI RxSBI	70–76	In/Out DDRSBI ($0112) for PSBI[5:2] TxSBI Out RxSBI, DIVBYP In	**Byteflight™** subsystem with Tx output, Rx and divider bypass input and general-purpose I/O on PSBI[5:2].
Port E PE[7:0]	26–29, 35–38	PE[1:0] In PE[7:2] In/Out DDRE ($0009)	**Mode selection**, **bus control** signals and **interrupt service request** signals; or general-purpose I/O.
Port P PP[7:0]	79, 80, 1–6	In/Out DDRP ($0057)	General-purpose I/O. PP[3:0] are use with the **pulse-width modulator** when enabled.
Port S PS[7:0]	68–61	In/Out DDRS ($00D7)	**Serial communications interface** and **serial peripheral interface** subsystems and general-purpose I/O.
Port T PT[7:0]	16–12, 9–7	In/Out DDRT ($00AF)	General-purpose I/O when not enabled for input capture and output compare in the **timer** and **pulse accumulator** subsystem.

Port Pull-Up, Pull-Down and Reduced Drive

MCU ports can be configured for internal pull-up. To reduce power consumption and RFI, the pin output drivers can be configured to operate at a reduced drive level. Reduced drive causes a slight increase in transition time depending on loading and should be used only for ports which have a light loading. Table 8 summarizes the port pull-up default status and controls.

Table 8 Port Pull-Up, Pull-Down and Reduced Drive Summary

Port Name	Resistive Input Loads	Enable Bit			Reduced Drive Control Bit		
		Register (Address)	Bit Name	Reset State	Register (Address)	Bit Name	Reset State
Port A	Pull-up	PUCR ($000C)	PUPA	Disabled	RDRIV ($000D)	RDPA	Full Drive
Port B	Pull-up	PUCR ($000C)	PUPB	Disabled	RDRIV ($000D)	RDPB	Full Drive
Port E:							
PE7, PE[3:0]	Pull-up	PUCR ($000C)	PUPE	Enabled	RDRIV ($000D)	RDPE	Full Drive
PE[6:4]	None	—			RDRIV ($000D)	RDPE	Full Drive
PE[6:5]	Pull-down	Enabled During Reset			—	—	—

Table 8 Port Pull-Up, Pull-Down and Reduced Drive Summary

		Enable Bit			Reduced Drive Control Bit		
Port P	Pull-up	PWCTL ($0054)	PUPP	Disabled	PWCTL ($0054)	RDPP	Full Drive
Port S	Pull-up	PURDS ($00DB)	PUPS0	Disabled	PURDS ($00DB)	RDPS0	Full Drive
PS[3:2]	Pull-up	PURDS ($00DB)	PUPS1	Disabled	PURDS ($00DB)	RDPS1	Full Drive
PS[7:4]	Pull-up	PURDS ($00DB)	PUPS2	Disabled	PURDS ($00DB)	RDPS2	Full Drive
Port T	Pull-up	TMSK2 ($008D)	PUPT	Disabled	TMSK2 ($008D)	RDPT	Full Drive
Port SBI:							
DIVBYP	Pull-down	Always enabled			—		
PSBI[5:2]	Pull-up	PCTLSBI ($0110)	PUESBI	Disabled	PCTLSBI ($0110)	RDRSBI	Full Drive
TxSBI	None	—			—	—	Full Drive
RxSBI	Pull-up	—	—	Enabled	—		
Port AD	None	—			—		
BKGD	Pull-up	—	—	Enabled	—	—	Full Drive